WMA -5

Heterogeneous Integration for WLP RF Transceivers : Challenges and Issues

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United Monolithic Semiconductors

Outline

- UMS motivation & strategy
- Heterogeneous Integration applied to RF Front End in mmWave
- SMART3 – System in Package deployment
- Conclusion

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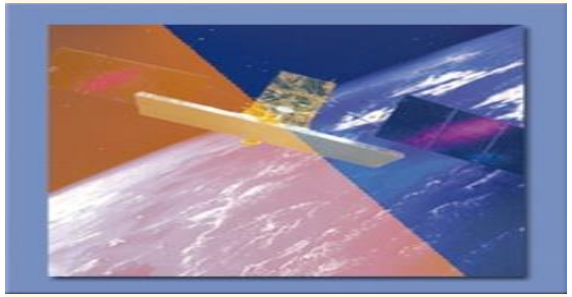
UMS offer, markets & technology platform

DEFENCE & SECURITY

- Phased array radar
- Electronic warfare
- Security applications

SPACE



- Communication satellites
- Earth observation
- Scientific mission

AUTOMOTIVE & SENSORS

- 24/79GHz short range radar
- 77GHz long range radar
- Sensors/road tolling

TELECOM

- Point to point radio links
- VSAT terminals
- Base stations

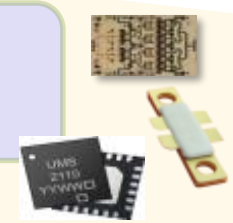
OFFER

FOUNDRY SOLUTIONS

- Wafers & services
- Packaging services
- Known good die and packages

PRODUCT SOLUTIONS

- RF MMICs ASICs & standard products
- Die and packaged products
- Multi-chip modules



TECHNOLOGY PLATFORM

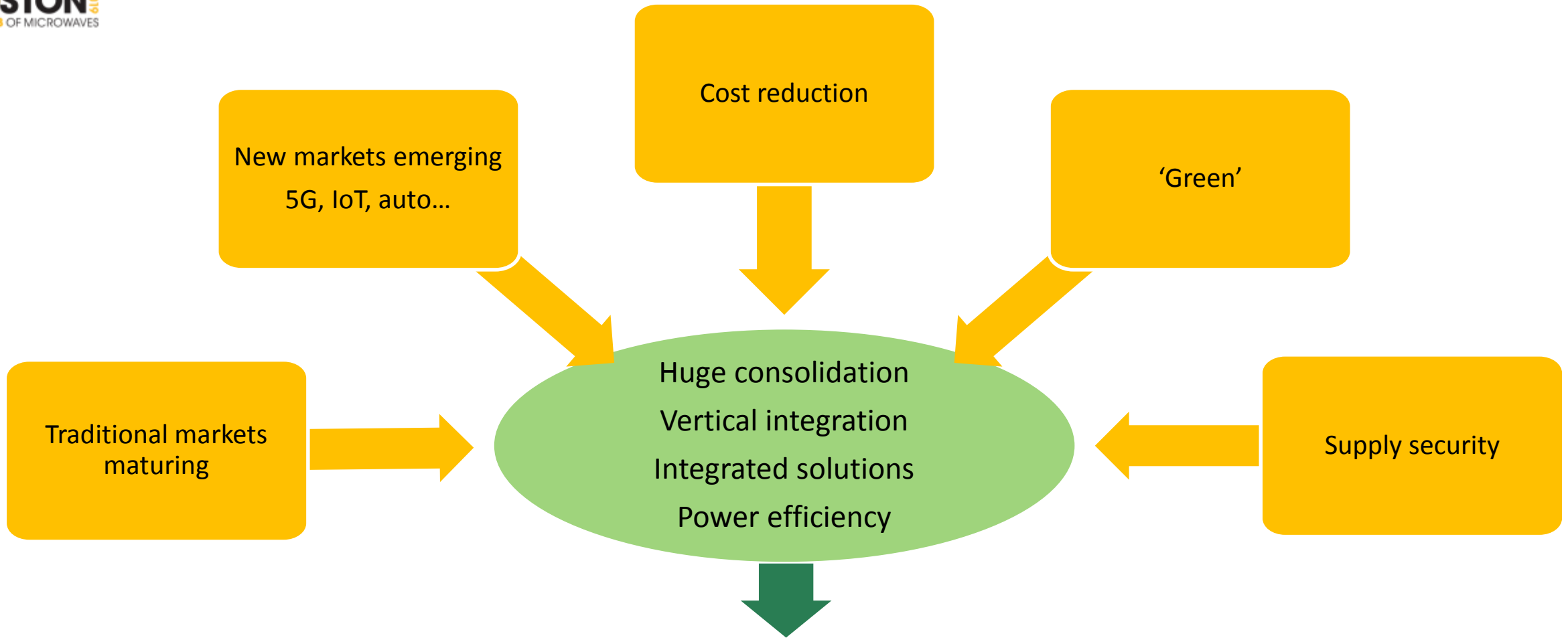
INTERNAL FOUNDRY
- European, ITAR free
- GaAs & GaN technology
- specialised

EXTERNAL FOUNDRY
- GaAs & SiGe technology
- High volume needs
- Commercial applications

PACKAGING
- Internal specialised
- High volume QFN
- Hermetic and power

COMPETENCE NETWORK
- Analysis capability
- R/D Institutes
- partnerships

Industry macro trends



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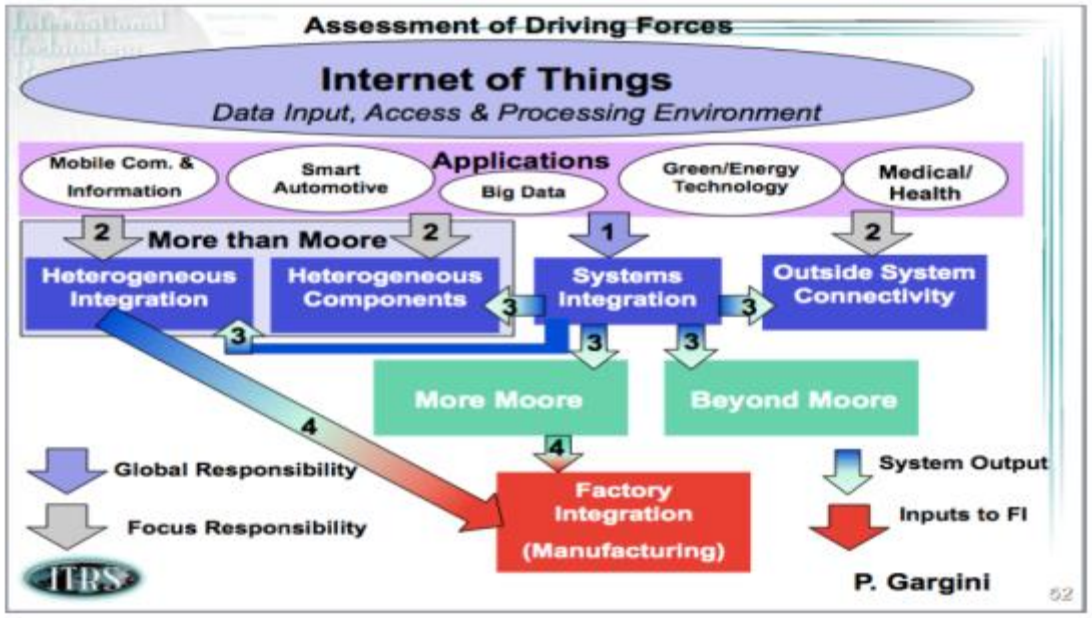
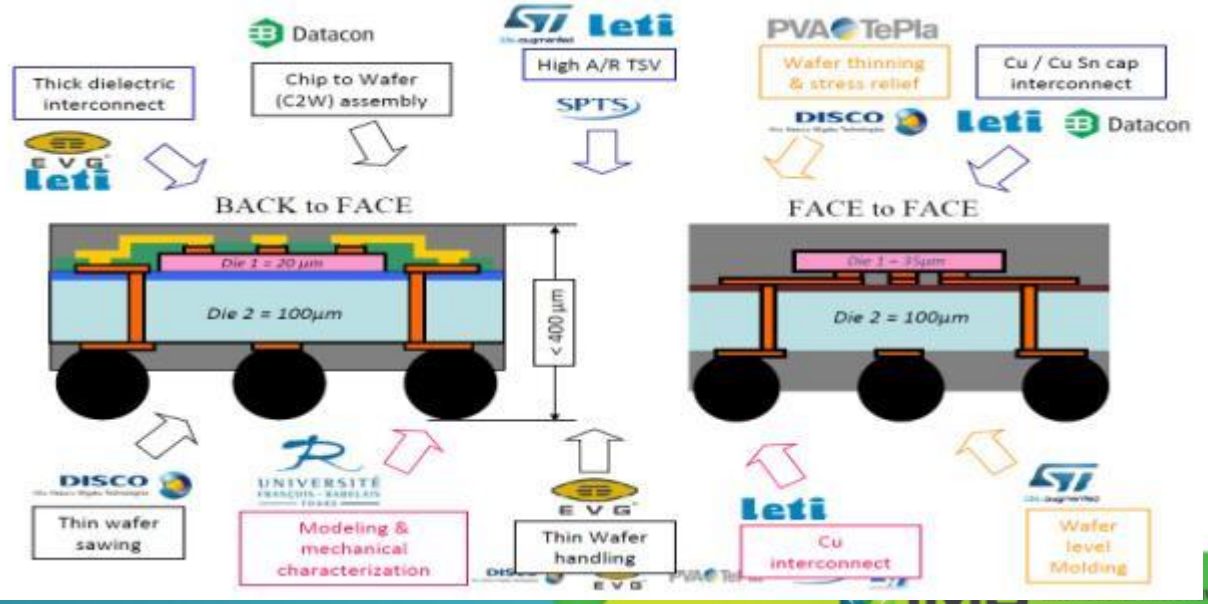
Heterogenous integration applied to RF Front End up to Millimeter Wave ...

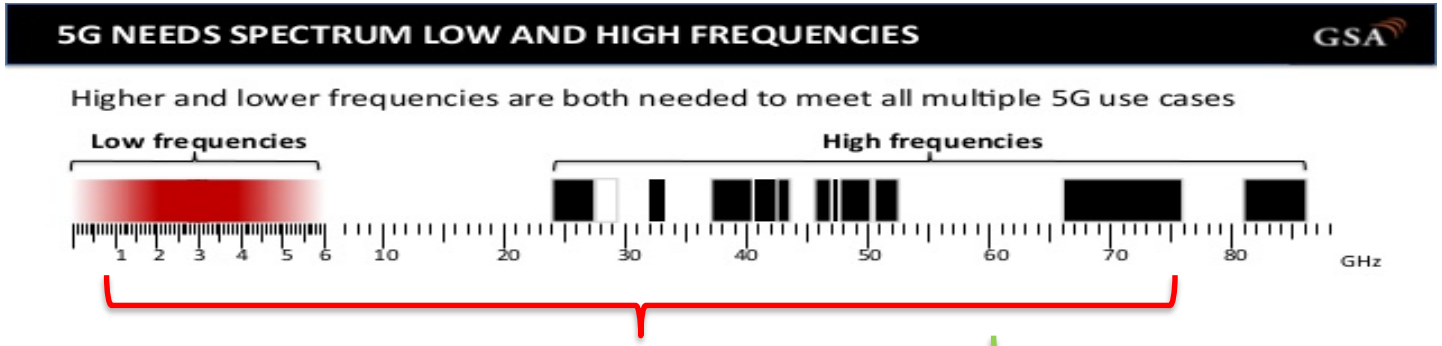
- **What Is Heterogeneous Integration ?**
- **Related to the Integration of multiple bare die ICs, based on differing substrate materials and process technologies, into a single carrier (package/module).**
  - Size : from 0.1 to x mm
  - Thickness : from 50 to 150 µm
- **Technologies: GaAs, InP, GaN, CMOS, etc., and Process nodes: 32nm, 28nm, 16nm, 10nm,**
  - Side-by-side, stacked, flip-chip, wire-bonded, WLP, MEMS, IPDs, etc.
- **Currently the most common method of integration is based on MCM/SiP technology**
- **Common platform for III-V device integration when Si cannot meet performance objectives**
  - Power
  - Noise
  - Losses

ITRS 2.0 – version 2014



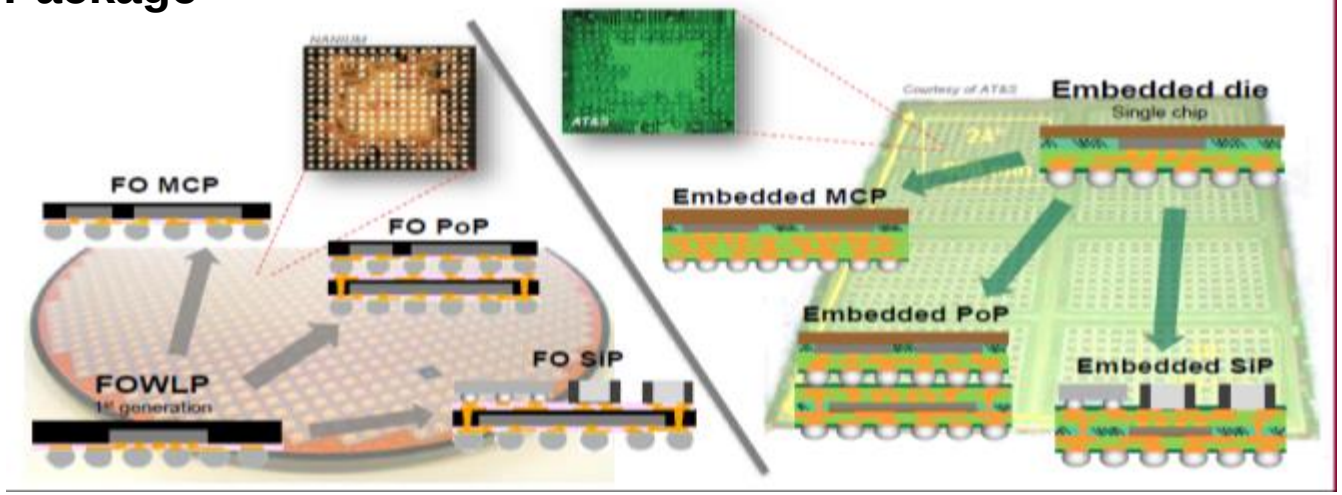


Wafer Level Packaging vs Panel Which domain for mmWave ?



Full Antenna at Wafer Level

System in Package



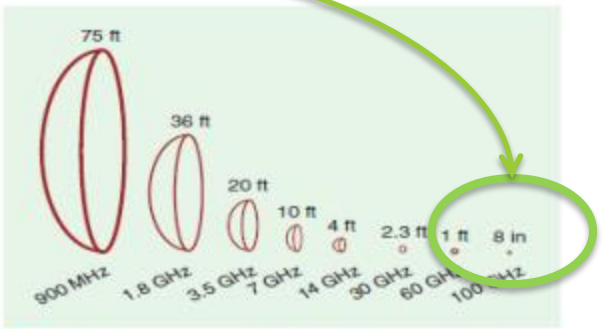
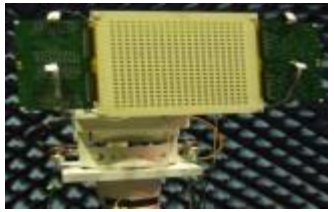


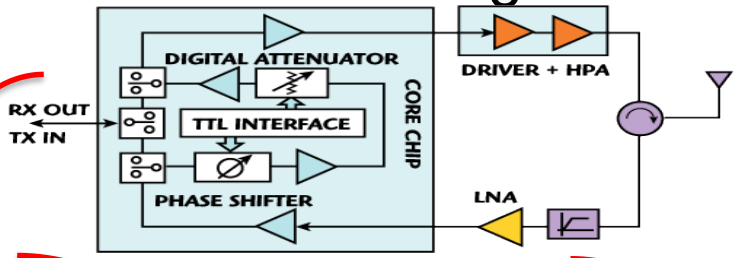
Figure 1. *Antenna size needed to produce a 1° beam width. An antenna with a 1° beam width and 50% efficiency has a gain of 44 dB [13], [14]. (Used with permission from Gigabeam.)*

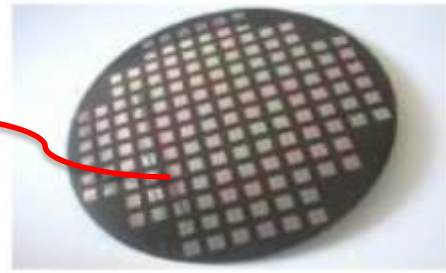
Trigger : Active Antenna concept / MiMo

- Need to integrate more and more complexity at Antenna level but footprint, weight and new applications are driving this demand

5G, Pt to Pt







Autonomous vehicles

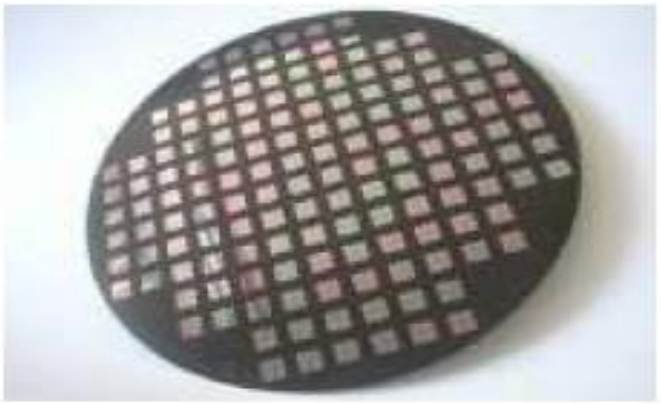
Space,
Constellations

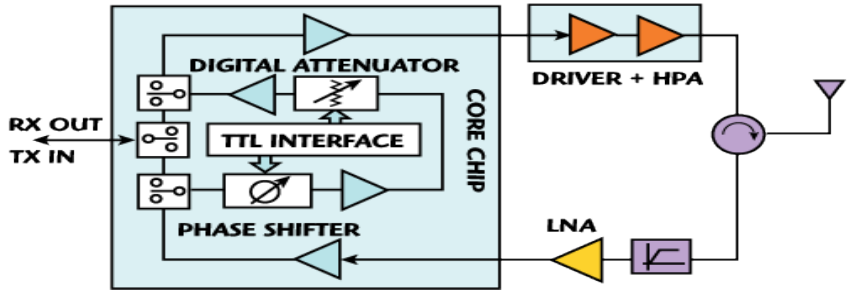
Defence

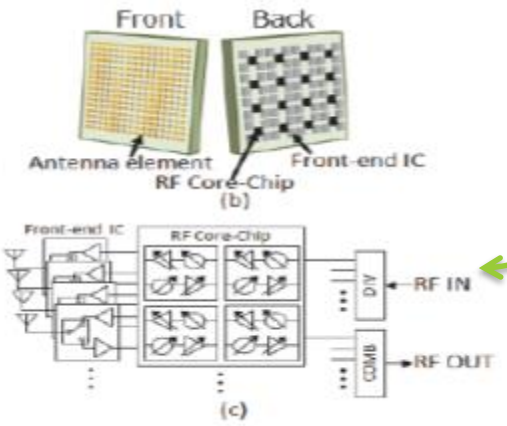
Sensors for Industries

Trigger : Active Antenna concept / MiMo

- **Need to integrate more and more complexity at Antenna level but footprint, weight and new applications are driving this demand**

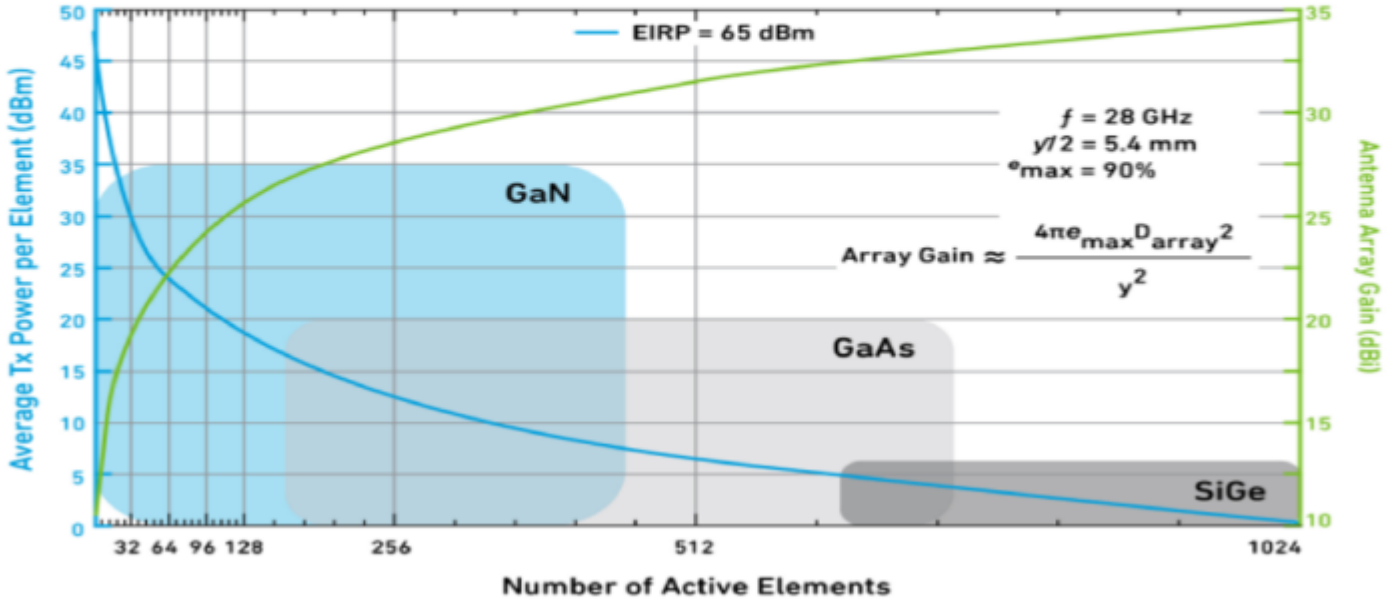






5G & Heterogeneous integration

- Trade off between the number of active elements
  - PA power/channel reduces as number of elements increases for a given EIRP
  - Beamforming circuitry becomes larger and more complex
  - With enough elements is SiGe a good choice?

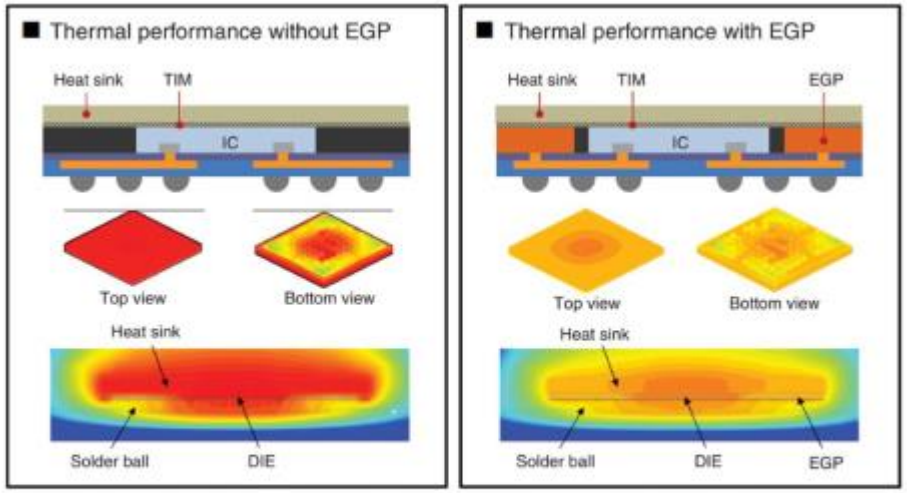


Wafer Level Packaging Technologies – Fan-out based

- Many variants developed for WLP. What are the specific technical items specific to RF Front End, this platform should address ?
- Frequencies : from to C to E Bands ... (D ??)
- Dissipated Power : up to 30W CW ➔ roughly 10 x 10 mm2 of footprint
- Max Surface : up to 15 x 15 x 0.5 mm2
- 3D compatible for Digital / RF integration ➔ PoP or double RDL approach
- Improved cooling by one side
- Hermetically compatible
- Shielding & Isolation in between channels by appropriate metallic protection
- 125°C Back Side / MTF 20 years

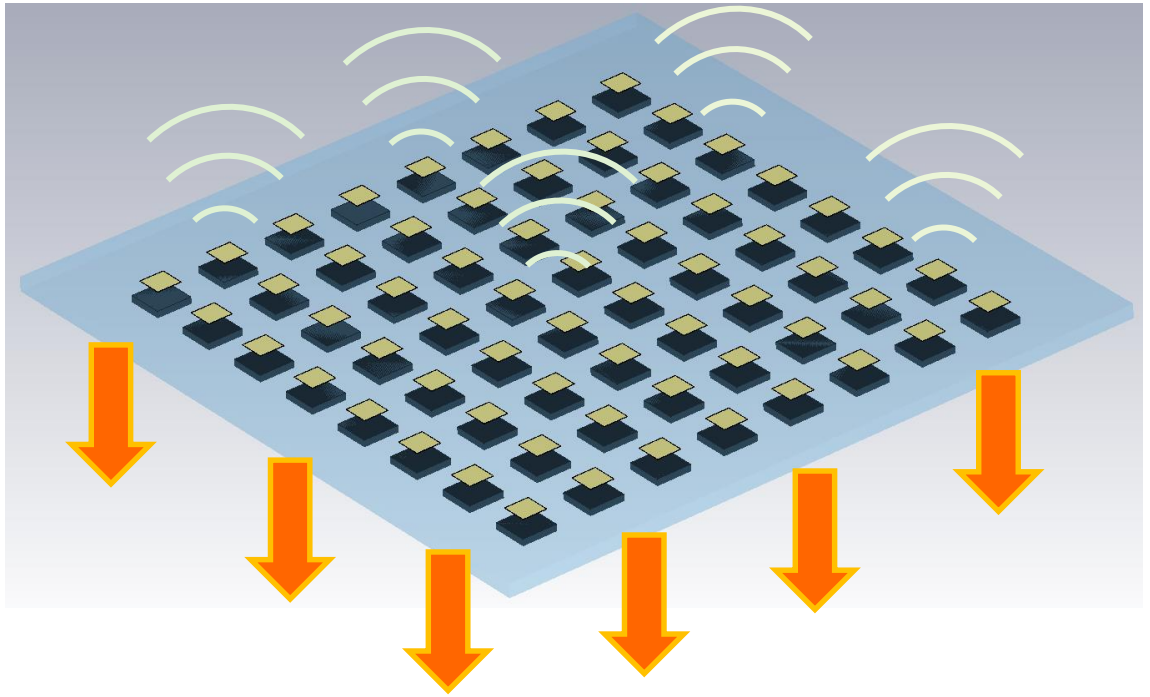
Thermal management for active antenna systems

- Antenna transmission on one side of the PCB
- Thermal dissipation on the other side of the PCB
  - ➔ Less complex PCB design
  - ➔ Cost efficient PCB
  - ➔ Compatible with mesh size

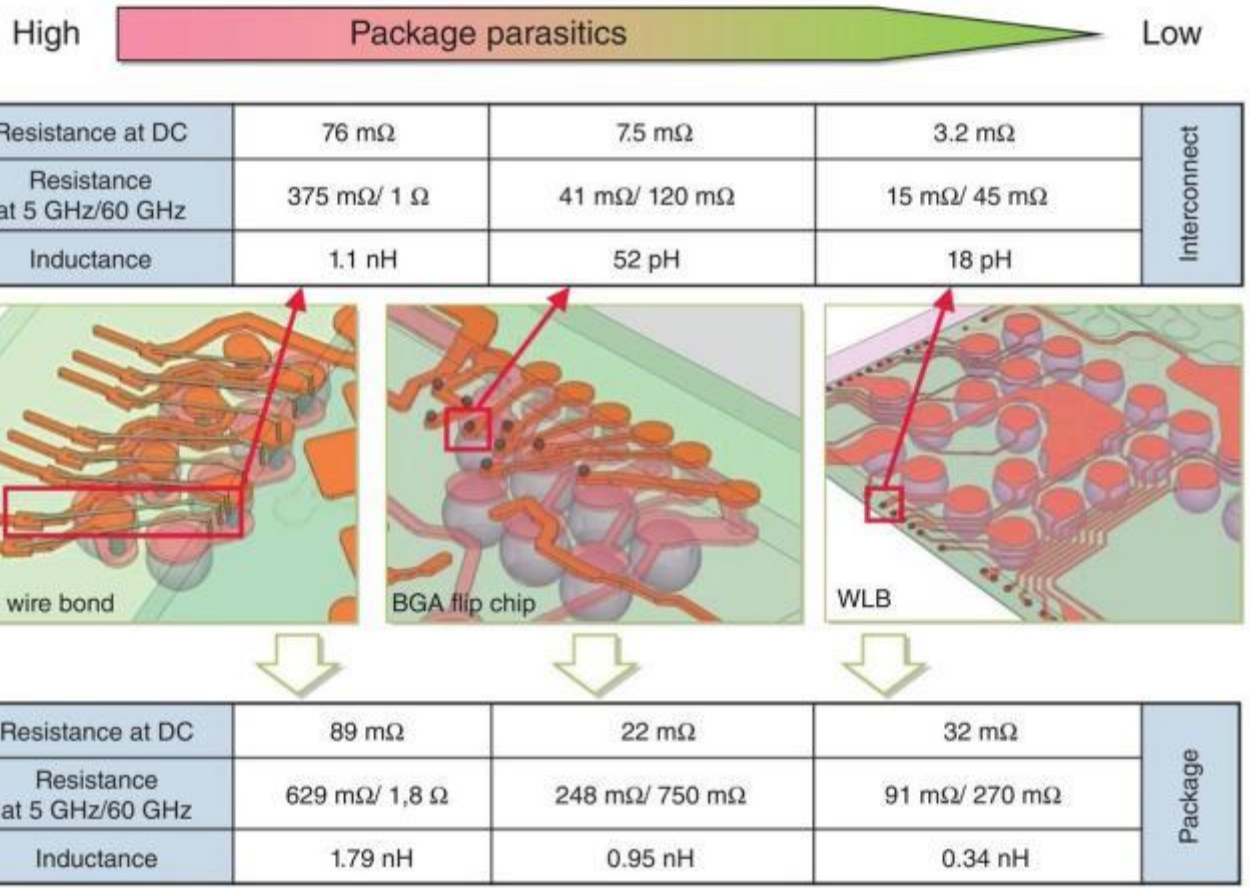


Type	Theta Ja	Theta Jb	Theta Jc	Remark
Type 1	46.0 K W^{-1}	18.37 K W^{-1}	7.13 K W^{-1}	TIM material : polymer
Type 2	34.4 K W^{-1}	13.87 K W^{-1}	6.80 K W^{-1}	TIM material : polymer

Array antenna module

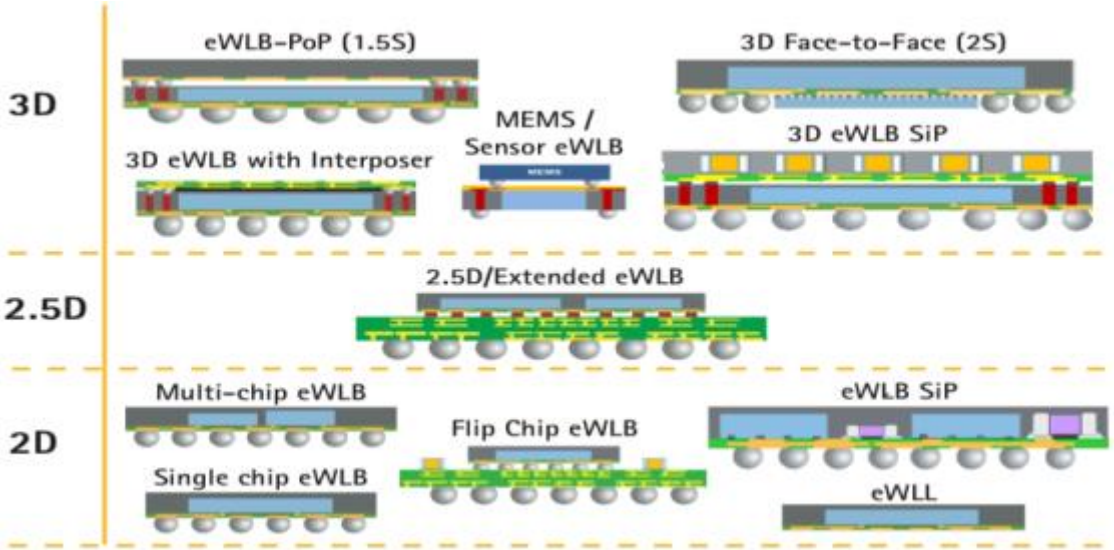


WLP and parasitic reduction

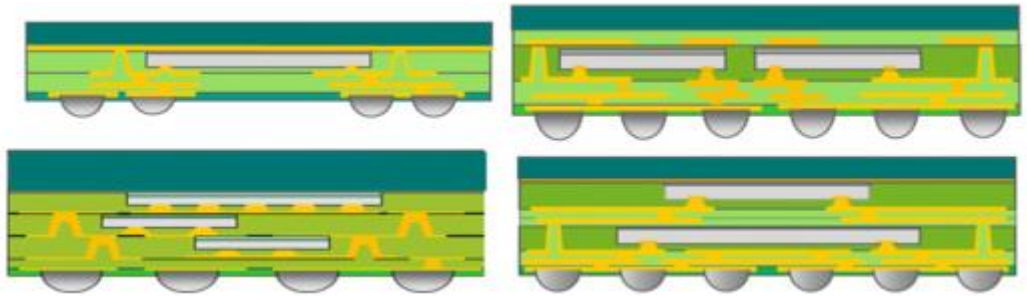


Wafer Level Packaging Technologies – Fan-out based

- **Many approaches and variant developed for WLP.**
- **Examples (among many ...)**



(**eWLB product portfolio Source: STATS ChipPAC**)



(EDS technology from Infineon)

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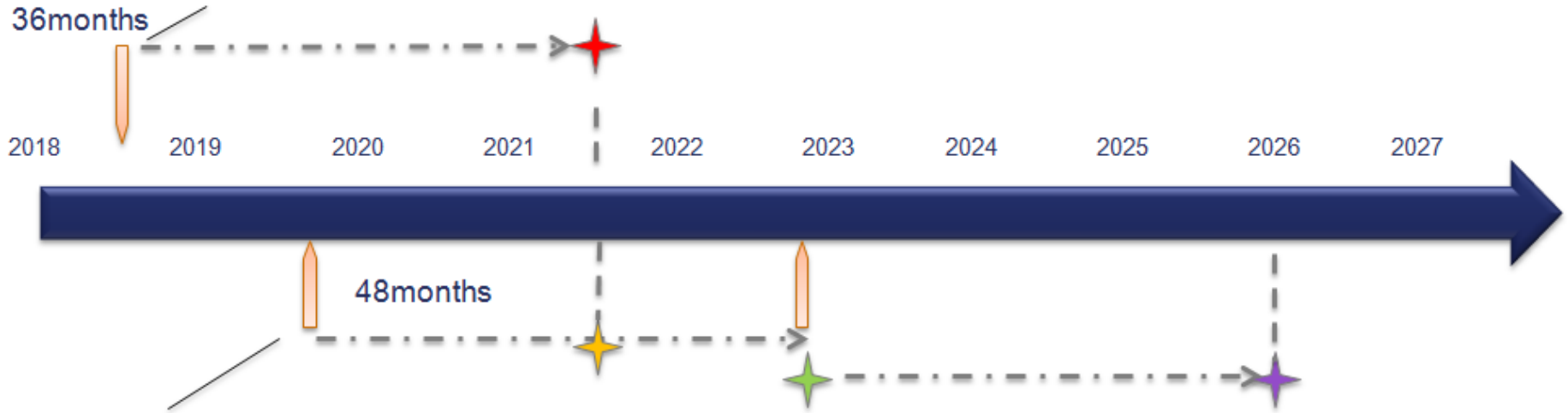
SMART3 – SIP Technology development

5G_GaN2
(Ecsel-RIA Eu + National)



SMART3 – R&D / 2022 Nanoelectronic Plan
- Notification Q3 2019

5G_GaN2
- R&D development

SMART3
-Technology optimization on R&D Lines
-Decision for transfer & process adaptation
- Qualification – Start in production

Ramp-up Milestone – Mass volume capabilities

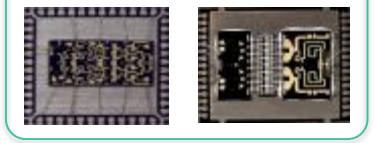
Qualification Milestone – Commercial application -

Scenario for industrialization - Transfer

Prototyping Milestone

Developments – Plastic Packaging roadmap

QFN/DFN plastic
Power - pulsed



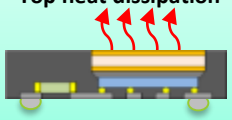
Thermal dissipation
by the top

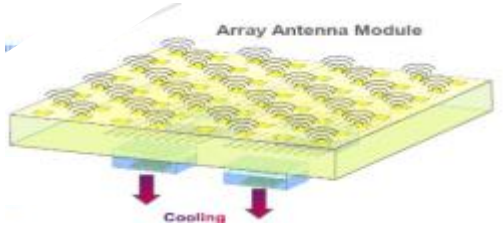
Inverted BGA power package
Top heat disspation

Development in progress (5G)

Cost reduction

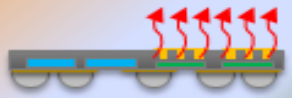
Inverted plastic power package
Top heat dissipation



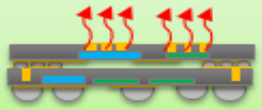


Power

SIP Fanout WLP
Heterogeneous integration
Backside cooling



PoP SIP Fanout WLP
Heterogeneous integration
Backside cooling



2.5D
Integration

5G-GaN2 Program

3D
Integration

SMART3

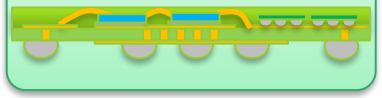
Integration

Current mutichip QFN solutions
GaAs-SiGe / 2 dies

Multichip QFN
GaAs-SiGe-GaN
Up to x dies

QFN pushed
Up to the limit

SiP BGA
GaAs-SiGe
> 10 dies

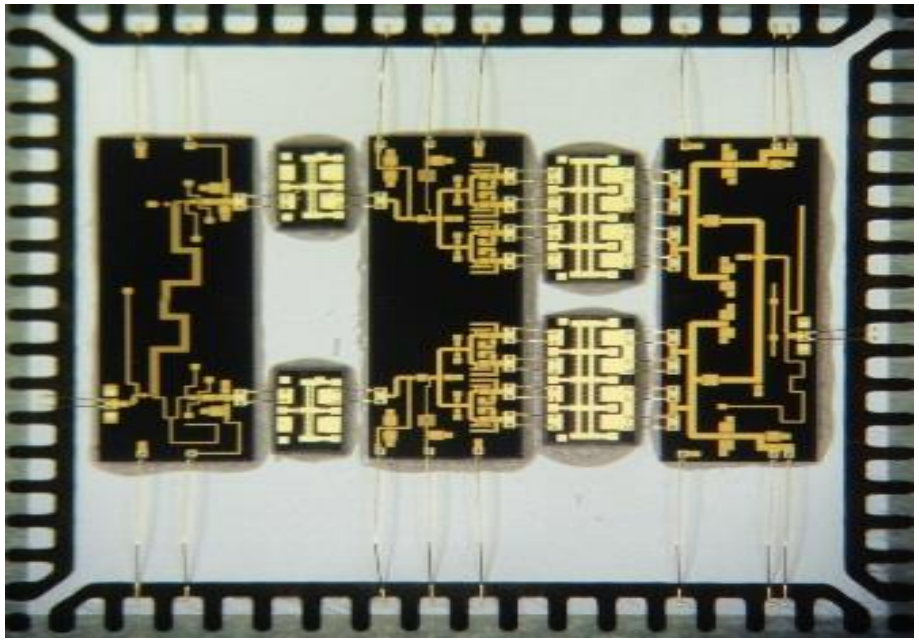


More I/O
Capability

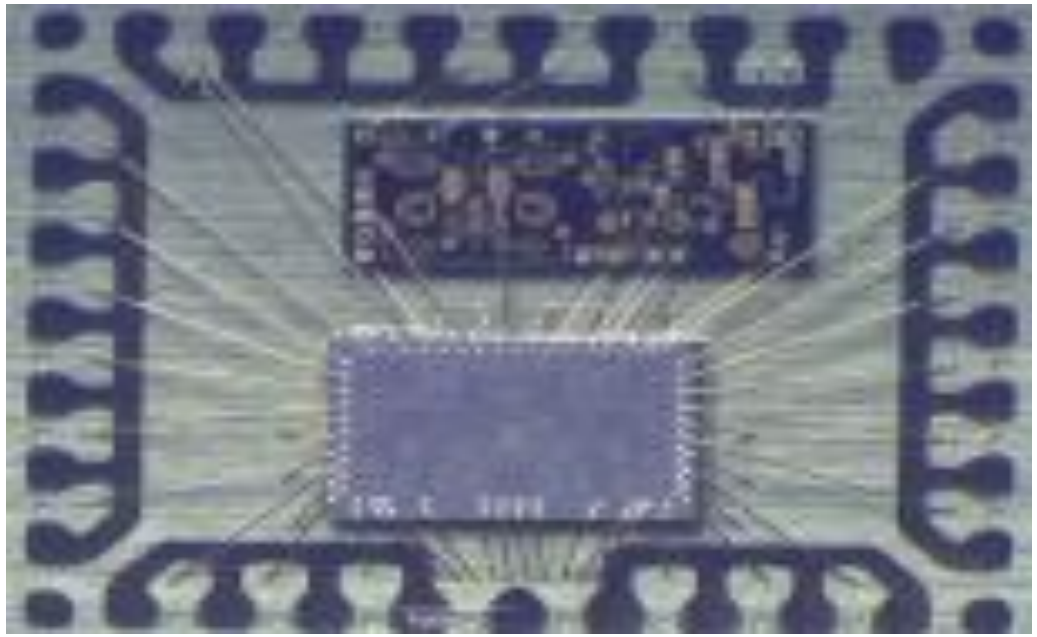
Development in progress (D&S)

Current solutions	2017	2018	2019	2020	2021	2022	2023	2024	2025+

Intermediate generations : Examples of UMS mixed technology solutions



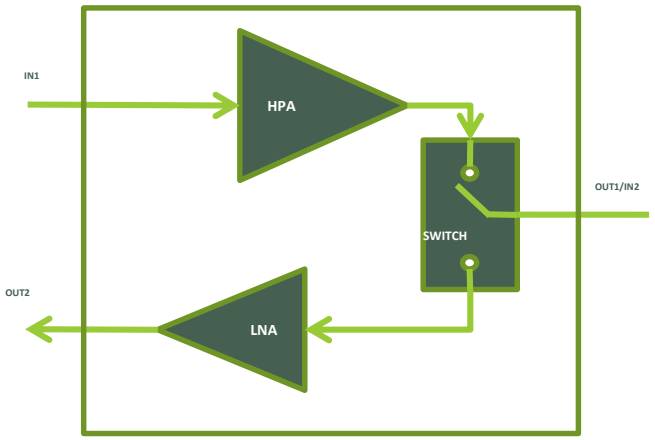
Advanced telecom PA
GaAs & GaN – 28 GHz

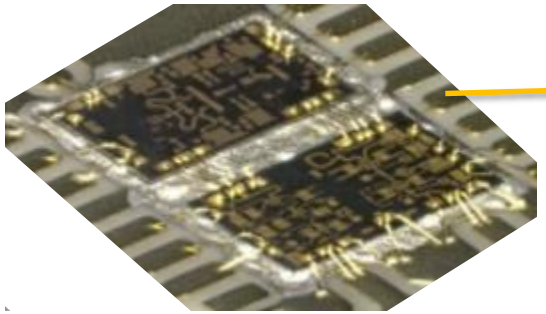


Automotive transceiver
GaAs & SiGe – 24 GHz

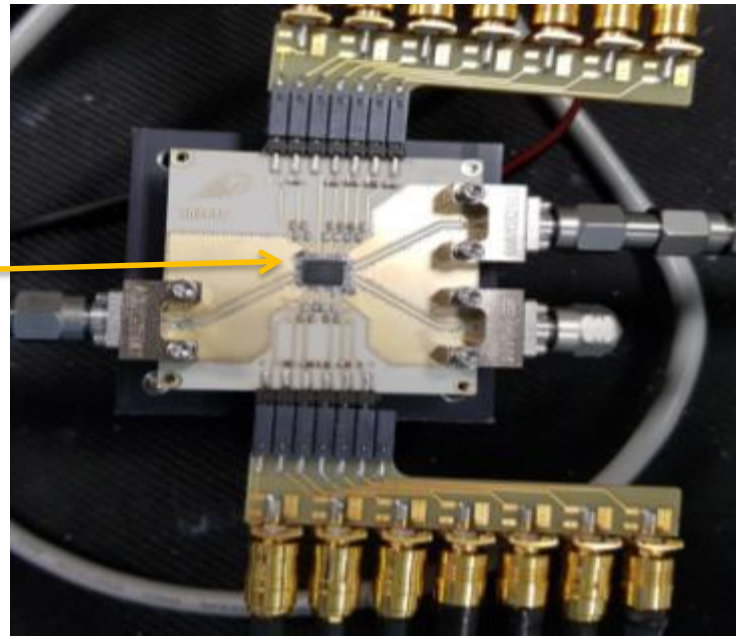
Intermediate generations : 5G 28GHz T/R solution

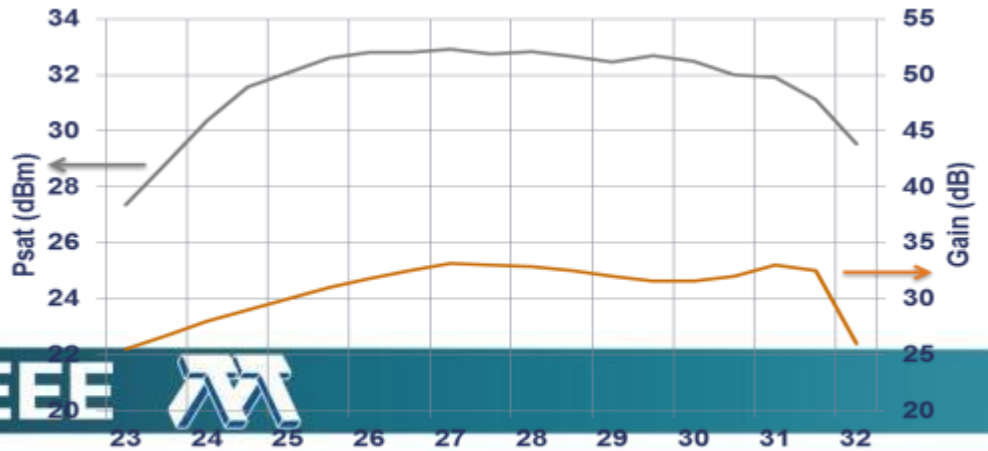
GaN/GaAs solution

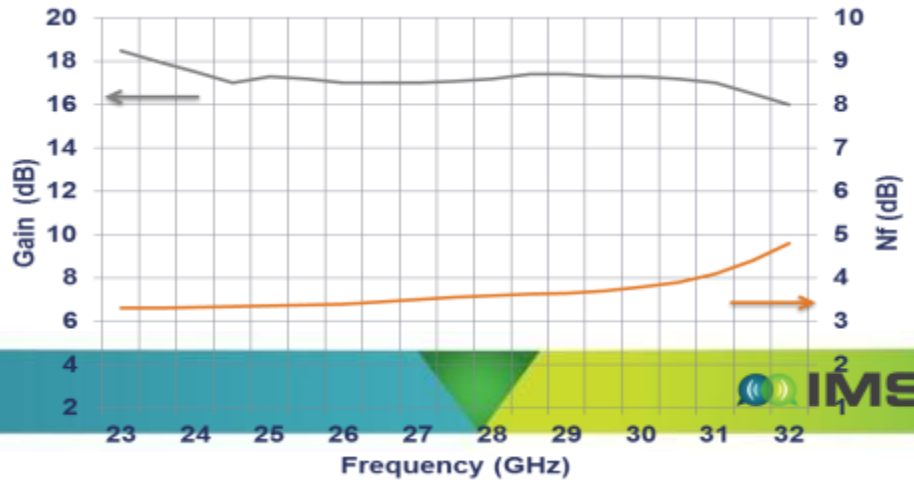




QFN4X5 on board





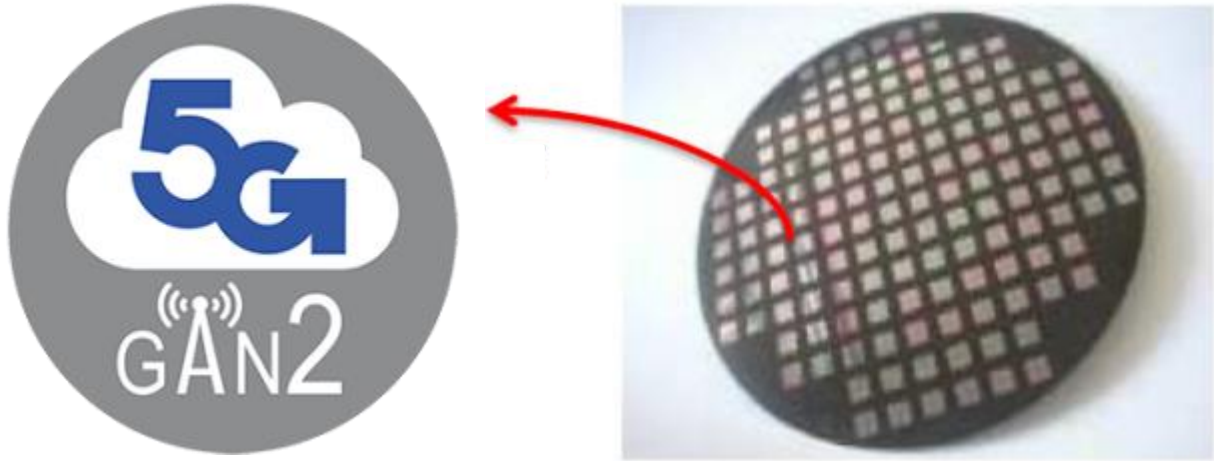


Next steps for 5G & System In Package

Heterogeneous Integration: Wafer Level Packaging

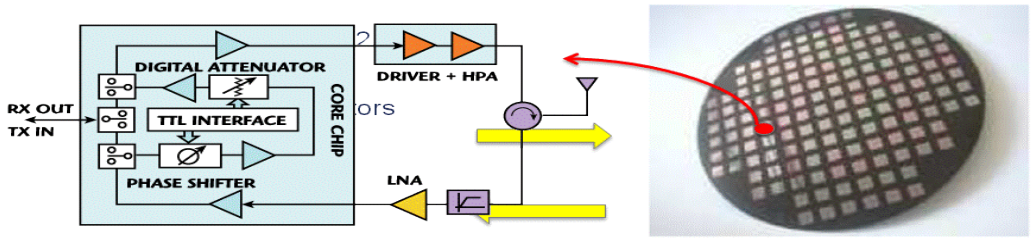
- Compact RF Front End multi-technology demonstrators covering 28, 39 and 80 GHz based on innovative Wafer Level Packaging integration.

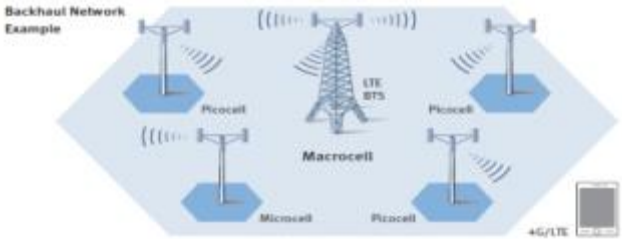
This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 783274. The JU receives support from the European Union's Horizon 2020 research and innovation programme and France, Germany, Slovakia, Netherlands, Sweden, Italy, Luxembourg, Ireland.".

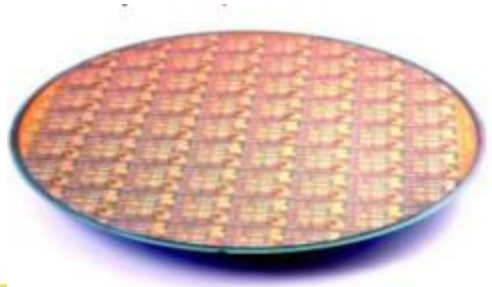


5G_GaN²

- **Three Domains**
  - 3D advanced co-integration of Si / GaN power technologies System in Package (SIP)
    - → TRL 5 to 6 in final
    - 70% program effort
  - Millimeter wave GaN Technology for E-Band Radio
    - → TRL3 to 4 in final
    - 15% program effort
  - Ka-Band GaN compatible of 8” RFCMOS fab line for high density RF / mass market transceivers
    - → TRL3 to 4 in final
    - 15% program effort





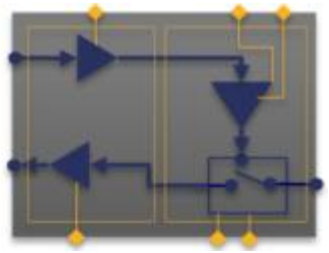


5G_GaN2

- **5G_GaN2 collaborative Project**
  - GaN & Packaging solutions for 5G
  - https://www.5ggan2.eu/
  - 17 European partners
  - **UMS as project coordinator**
  - 3 years project 2018-2021

Demonstrators for 5G BTS 28GHz & 39GHz

- SiP FOWLP package technology
  - ✓ Top side cooling topology
  - ✓ Integration / Miniaturization



Coordinator United Monolithic Semiconductor SAS

3-5 Lab

Benetel

CEA Leti

Ericsson

Fraunhofer Institute of Applied Solid-state Physics (IAF)

MEC

Molecular plasma group former Funcoats

Sencio

Slovak University of Technology in Bratislava

Swegan

Tesat Spacecom

Thales CS

United Monolithic Semiconductor GmbH UMS

University College Dublin

University of Padova

X Fab Semiconductor

IPCEI : Important Project of Common European Interest

Authorization to Proceed
(Respect of competition rules)

France - 7 projects (Plan nano 2022)

1. **UMS - SMART 3**
2. STm
3. XFAB
4. SOITEC
5. SOFRADIR
6. MURATA (ex IPEDIA)
7. ULIS

DGE DIRECTION GÉNÉRALE DES ENTREPRISES

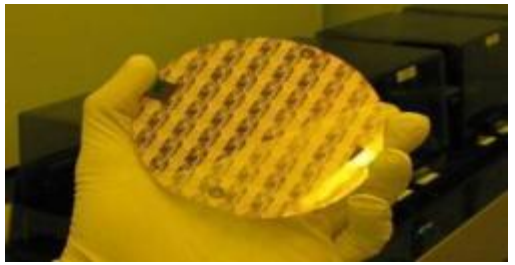
DGA

SMART3
- Lyon University (Polymer, packaging)
- Bordeaux University (Design, Reliability)
- Limoges University (Complex simulation,Design, Test)
- Linxens (Packaging development)
- Nokia (Demonstrator)
- CEA LETI (Packaging development)
- 3-5 lab (Packaging, GaN E Band)
- Thales DMS (Packaging support & specifications)

SMART3 - Activities

- WLP Technology development and assessment
  - Polymer formulation and adaptation
  - Compatible of High T° / CTE /
- Modelling
  - EM 3D, Thermo-mechanical, Electrical ➔ PDK
- Reliability
  - Evaluation, Pre-qualification
- Demonstrators
  - 5G in Ka Band, V-Band, E-Band

GaN technology and WLP compatibility



0.50 µm (GH50) — 2011 (3”) → Moving to 4” → Space evaluation In progress

0.25 µm (GH25) — 2014 (4”) → Running in production and Space evaluated

VHF	UHF	L	S	C	X-Ku	K	Ka	Q	V	E

30 MHz — 4 GHz — 8 GHz — 30 GHz — 50 GHz — 90 GHz

-Copper based (RDL) for interconnection and cooling
-- Hotvias

0.15 µm (GH15) — Early access mode since beginning of 2018 (4”)

Production & Space listed

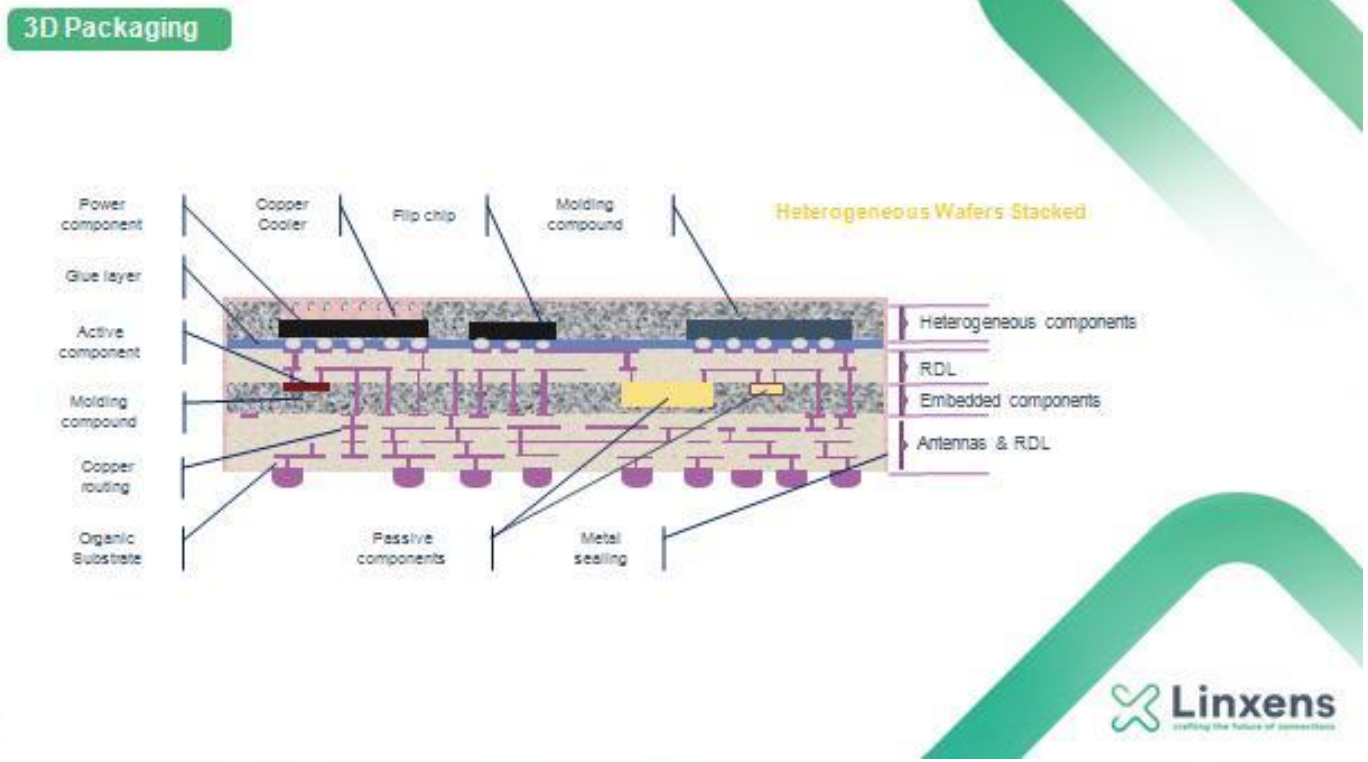
Production

Development

0.10 µm (GH10) — Released foreseen late 2020 (4”)

SMART3

- WLP technology applied to power and mixed Analog / Digital RF FE



SMART3 - Reliability

- **Test Vehicle by Building block of the WLP process**
- **Evaluate Mechanism of End of Life**
- **Associated to Energy of Activation**
- **Evaluate Maximum Ratings**

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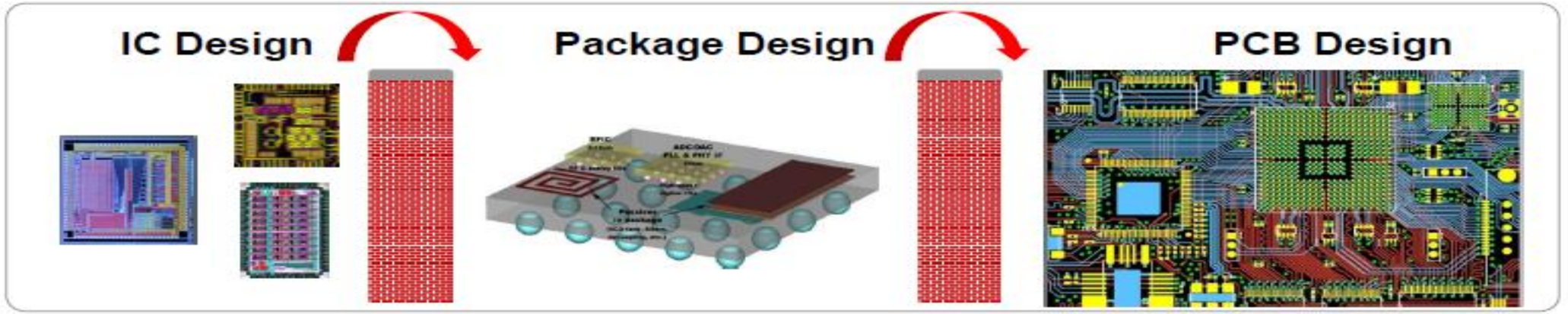
Stress test	Standard/spec	Pass criteria
Moisture sensitivity level (MSL)	EIA/J-STD-020C (Level 1)	MSL 1
High temperature storage (HTS)	JESD22-A103 (Ta: 150 °C)	1000 h
Temperature cycling (TC)	JESD22-A104 (Cond B: 55–125 °C) Preconditioned (Level 1; Tr: 260 °C)	1000× 1500×
Unbiased HAST (uHAST)	JESD22-A118 (Cond A: 130 °C/85% RH) Preconditioned (Level 1; Tr: 260 °C)	96 h 188 h
Temperature humidity bias (THB)	JESD22-A101 (85 °C/85% RH, VCC)	1000 h
Temperature cycling on board (TCoB JEDEC)	IPC 97-01 (−40 °C/+125 °C, 1 cy h^{-1})	500× 1000×
Temperature cycling on board	NOKIA spec.	FF > 500 cycles

SMART3 - Modelling strategy

- Standard approach – step by step but inappropriate



- ➔ Complete toolbox for co-design a complex SIP
- ➔ Develop a complex model approach

Outline

- UMS motivation & strategy
- Heterogeneous Integration applied to RF Front End in mmWave
- SMART3 – System in Package deployment
- Conclusion

Conclusions

- WLP as an extension of FE process / foundry offers
- Opportunity to design and produce a new generation of RF products
  - Integration / Performances / Cost / Supply chain
- SMART3 presents an alternative for low to medium volumes
  - Communication (5G, Backhauiling, ..
  - Strategic domains (Aerospace, Security ..)