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ANALYSIS OF THERMAL PROPERTIES OF POWER MULTIFINGER HEMT DEVICES

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ABSTRACT

In this paper, several methods suitable for real time on-chip temperature measurements of power AlGaN/GaN based high-electron mobility transistor (HEMT) grown on SiC substrate are presented. The measurement of temperature distribution on HEMT surface using Raman spectroscopy is presented. We have deployed a temperature measurement approach utilizing electrical *I-V* characteristics of the neighboring Schottky diode under different dissipated power of the transistor heat source. These methods are verified by measurements with micro thermistors. The results show that these methods have a potential for HEMT analysis in thermal management. The features and limitations of the proposed methods are discussed. The thermal parameters of materials used in the device are extracted from temperature distribution in the structure with the support of 3-D device thermal simulation. The thermal analysis of the multifinger power HEMT is performed. The effects of the structure design and fabrication processes from semiconductor layers, metallization, and packaging up to cooling solutions are investigated. The analysis of thermal behavior can help during design and optimization of power HEMT.

INTRODUCTION

Recent progress in GaN-based high-electron mobility transistors (HEMT) has confirmed them to be the main transistor technology for upcoming high-power devices at high-frequency operation because of their excellent electronic properties, especially high electron saturation velocity, and high breakdown voltage [1-4]. Multifinger devices with compact layout are required for high-power operation. However, self-heating induced thermal crosstalk between individual gate fingers can become a significant issue, which degrades device performance or can result in irreversible damage. Therefore, thermal management is crucially important to the viability of power HEMT [5-7].

Experimental temperature measurements are essential for complex characterization of these devices. Temperature is one of the dominant drivers of device degradation and has a substantial influence on the device. Therefore, it is very important to be able to accurately determine the device temperature in order to assess the reliability and performance. Among all techniques micro-Raman thermometry is one of the most popular for this purpose [8, 9], along with the electrical parameter-based thermometry [10]. Compared to an infrared technique with low spatial resolution of about 5 – 10 μm, the micro-Raman thermometry has spatial resolution better than 1 μm [11]. It can be used with advantage to profile micrometer sized source/drain openings in HEMTs. However, the micro-Raman technique can only be used for open or window packaged devices without metal air bridges between source/drain fingers or a source/gate field plate.

Another common approach to determine the chip temperature is by integration of on-chip sensors. Usually, the well-known temperature dependent characteristics of a pn junction are generally used in Si devices, e.g., [12-15]. It is highly sensitive and behaves mostly linearly, which is why pn junctions are often the temperature sensor of choice. For the GaN-based devices the Schottky diode can be used instead of the pn junction [16, 17].

In this paper we present the thermal analysis of multifinger power HEMTs. The effects of the structure design and fabrication processes from semiconductor layers, metallization, and packaging up to cooling assemblies are studied. The analysis is supported by 3-D device simulations as a highly useful and effective tool for the analysis and characterization of electrothermal behavior of power HEMTs. The material thermal

coefficients for the model are extracted and calibrated using different methods. The investigation uses micro-Raman spectroscopy and neighboring Schottky diode electrical measurement where the Raman shift and Schottky voltage at constant forward current are directly proportional to the temperature, respectively. The results are validated by micro thermistor measurement.

STRUCTURE DESCRIPTION

The structure under investigation is a 1.5 nm GaN-cap/ 14.5 nm $Al_{0.29}Ga_{0.71}N$-barrier/ 50 nm GaN-spacer/ 1650 nm GaN-doped heterostructure grown on 500 µm 4H-SiC substrate. Fig. 1 depicts the 2-D cross section of the structure. The backside 5 µm thick Au substrate contact is soldered to 1000 µm thick CuMo leadframe by a 25 µm thick AuSn solder. Top ohmic drain/source and gate contacts are created by Au-based metallization layers with thicknesses of 0.5 µm and 0.6 µm, respectively. The structure is set in open package which is placed on a cooler (Fig. 2).

METHODS FOR TEMPERATURE EXTRACTION

A gated transmission line method (GTLM) topology (Fig. 2) is used for electrothermal characterization. The first transistor (D1-G1-S1) in GTLM topology is used as the heat source. Several experimental methods are proposed and evaluated for extraction of structure temperature at different position.

Micro-Raman Thermometry

The MonoVista 750 CRS system with laser excitation wavelength of 514 nm was used for Raman spectra recording. In the first step, calibration measurements were done to obtain the Raman shift of GaN and SiC phonons as a function of absolute temperature (Fig. 3). These measurements were performed on a temperature-controlled chuck in a chamber. The measured GaN E_2 and 4H-SiC TO high phonon locations are ~568 cm^{-1} and ~776 cm^{-1} at room temperature, respectively [18]. An obvious exponential relation between Raman shift and

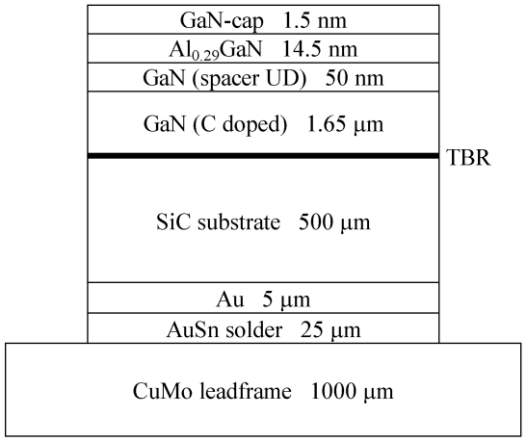


Fig. 1. 2-D cross section of the analyzed structures.

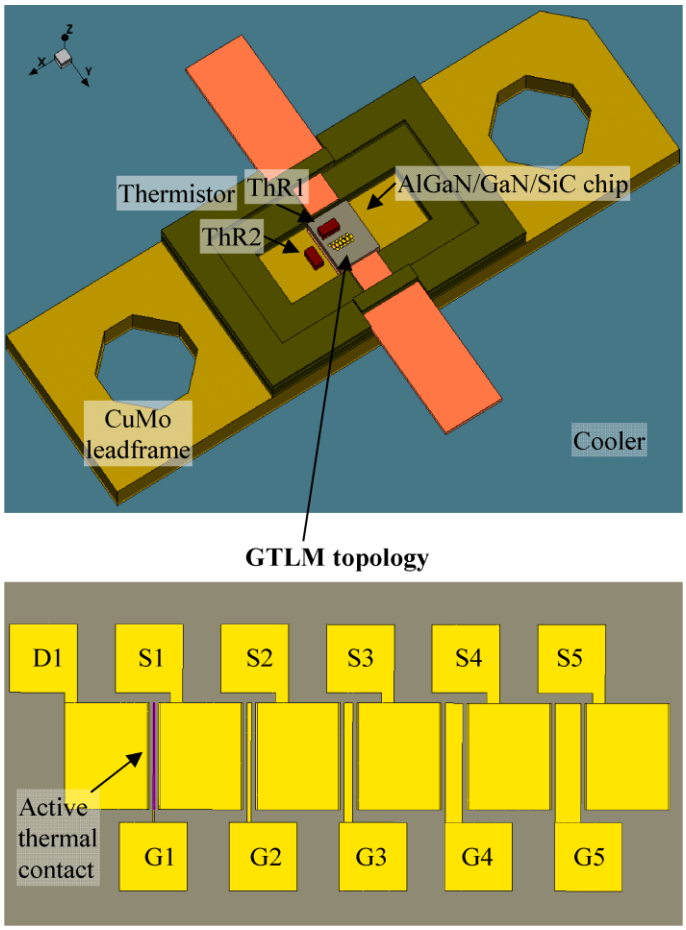


Fig. 2. 3-D thermal model of the structure with GTLM topology.

the temperature of the device is plotted in Fig. 4. This measurement was used as calibration for determination of the absolute temperature at specific locations of device under operation. Subsequently the measurements were performed at various locations for different dissipated power of the active

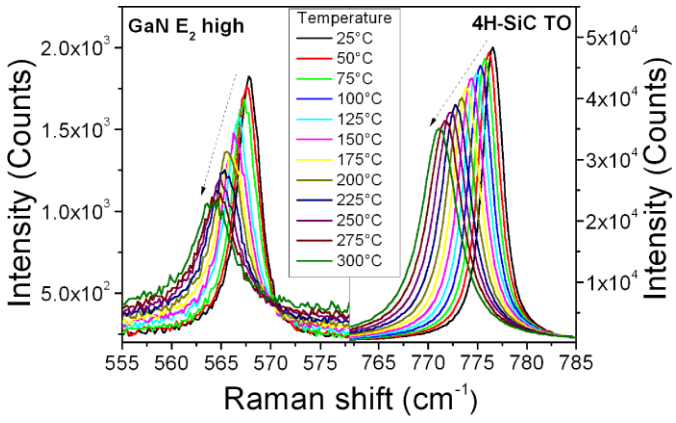


Fig. 3. Raman spectra of GaN E2 high phonon and 4H-SiC TO phonon at different temperatures.

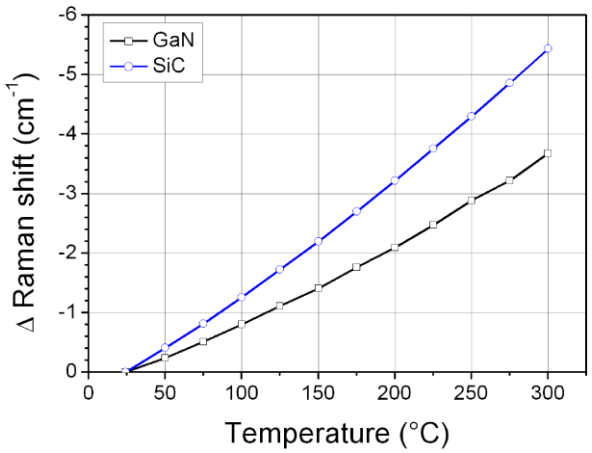


Fig. 4. Raman phonon peak shift dependence on the temperature.

HEMT device.

Schottky diode

This proposed method is based on temperature sensitive parameters of neighboring Schottky diodes to determine the device temperature at various positions. The first transistor (D1-G1-S1) in GTLM topology is used as the heat source. The rest of the transistors use only gates and sources to utilize the Schottky diodes (G2-S2, G3-S3, G4-S4, and G5-S5). In the first step, a calibration measurement of Schottky diodes at defined temperatures was performed (Fig. 5). The voltage difference for a constant current density of 0.1 A/cm^2 at forward bias is directly proportional to the temperature (Fig. 6). In the next step, the first transistor was connected to the power supply to generate heat. By applying the temperature calibration curve of the Schottky diodes we can obtain the temperature of the diodes at distinctive positions as a function of dissipated power.

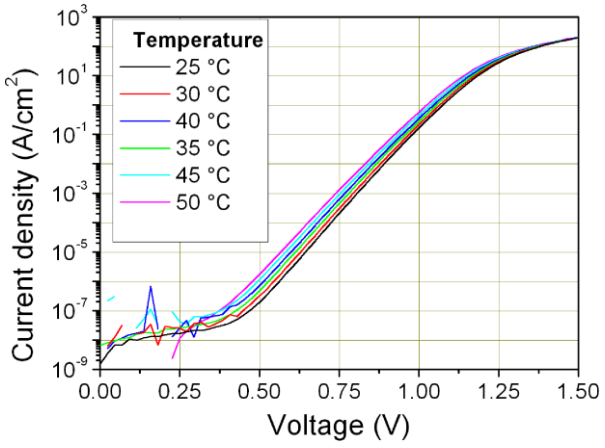


Fig. 5. Static *I-V* characteristics of the Schottky diode at different temperatures.

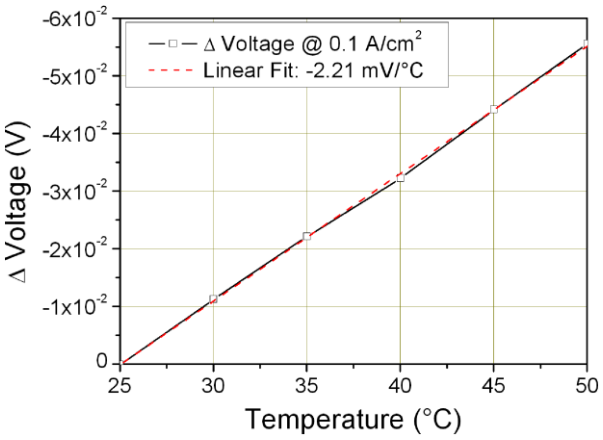


Fig. 6. Calibration curve of voltage deviation as a function of temperature.

Thermistor

MURATA NCP03WB473J05RL [19] micro thermistor was used for direct temperature evaluation of the device. The thermistor has a very high accuracy (~3 %). However, the thermistor dimension is large compared to the GTLM topology. Therefore, only one thermistor (ThR1) was attached on the chip near the active HEMT using thermal glue. A second thermistor (ThR2) was attached to the leadframe near chip. These thermistors were used to validate the above described methods and determine the heat transfer from chip to leadframe through the solder interface.

3-D MODEL DESCRIPTION AND EXPERIMENTAL VALIDATION

The 3-D model of the structure for thermal simulation based on the physical and geometrical description of all semiconductors, metallization layers, and package corresponding to the real device is created in Sentaurus Device Editor [20] (Fig. 2). 3-D thermal simulations are performed in Sentaurus Device tool [20]. A few nm thick GaN-cap and AlGaN barrier layer are neglected in the model due to their minimal impact on the thermal simulations. The thermal boundary resistance (TBR) is set to 1×10^{-4} cm^{2}KW^{-1} at the GaN/SiC interface [21]. TBR value of 2 cm^{2}KW^{-1} is set at the CuMo leadframe/cooler interface. The dissipated electrical power which results in thermal heating is modeled by a heat source placed under the gate electrode edge at the drain side, where the heat generation occurs during the on-state operation of the device [22, 23]. The device boundary conditions are set to account for the heat transfer to the surrounding environment. The thermal conductance value of 15 Wm^{-2}K^{-1} represents heat conduction to the air [24]. The material thermal coefficients for the structure model are taken from literature and calibrated using above described methods. The thermal conductivities of used materials are evaluated from measured temperature

distribution on the chip. The thermal coefficients for the materials in the structure are listed in Table 1.

Material	Thermal conductivity ($Wm^{-1}K^{-1}$)
Au	310 [25]
AlGaN	$40\times(T/298)^{-1.37}$ [26]
GaN (C doped)	$190\times(T/298)^{-1.37}$ [27]
4H-SiC	$430\times(T/298)^{-1.5}$ [28]
AuSn	57 [29]
CuMo	160 [30]

Table 1. Thermal conductivity values calibrated and used in the simulation.

Fig. 7 shows simulated structure temperature distribution for applied power 2 W in the active D1-G1-S1 HEMT. Fig. 8

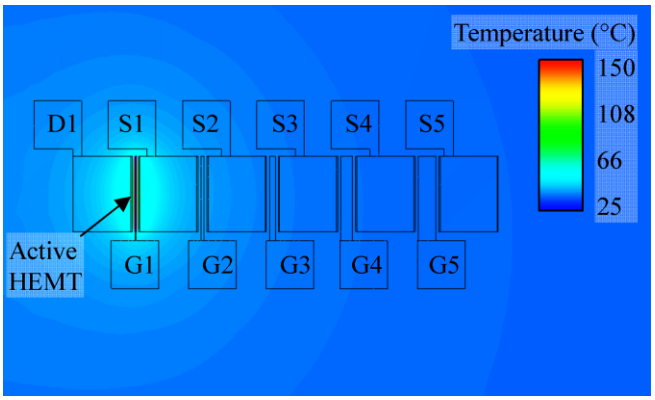


Fig. 7. Simulated temperature distribution in the structure for dissipated power of 2 W at the active D1-G1-S1 HEMT.

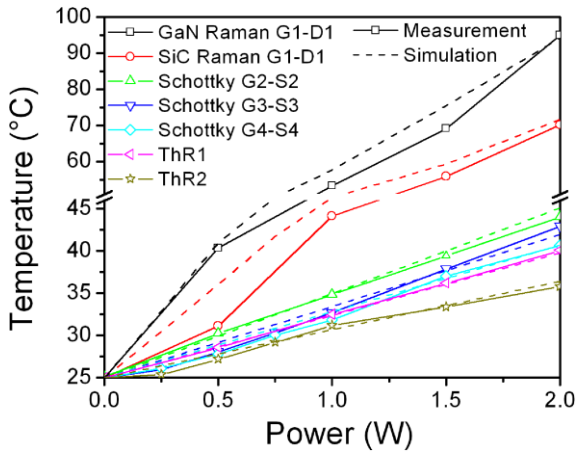


Fig. 8. Comparison of the measured and simulated temperatures of Raman G1-D1 position, Schottky contacts G2-S2 – G4-S4, and thermistors ThR1 and ThR2 at different powers of the active D1-G1-S1 HEMT.

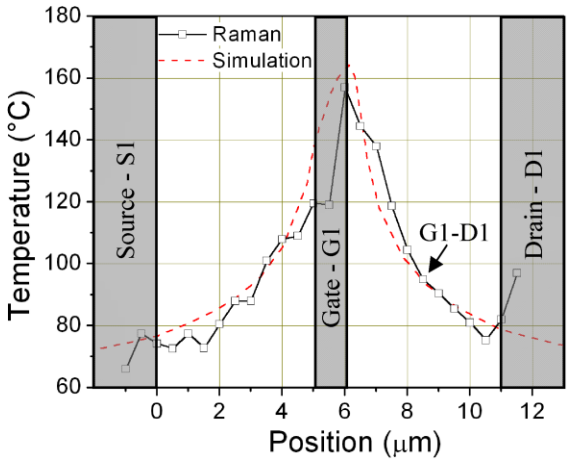
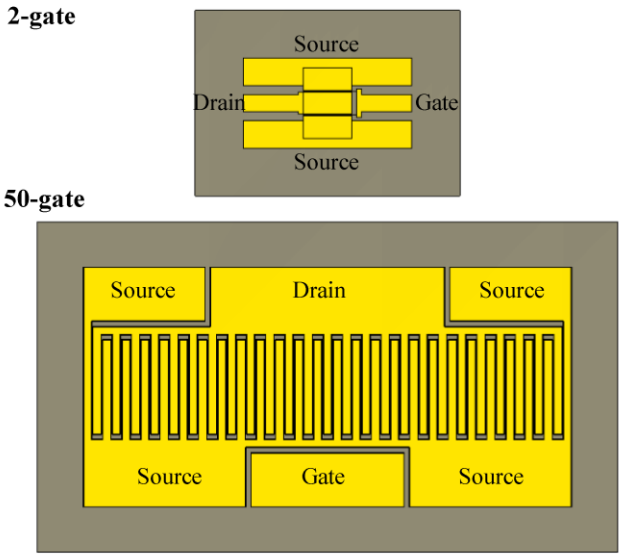


Fig. 9. Comparison of the measured and simulated temperature distributions across the active D1-G1-S1 HEMT for 2 W.

shows the comparison of measured and simulated temperatures of Raman G1-D1 position, Schottky contacts G2-S2 – G4-S4, and thermistors ThR1 and ThR2 at different powers of the active D1-G1-S1 HEMT. Fig. 9 shows the temperature distribution across the active HEMT. Only measured temperatures under HEMT electrodes (S1, G1, D1 - gray regions) show incorrect values because the Au-based metallization is not transparent for Raman excitation beam.



Number of elementary gates	2	50
Gate length	0.5 μm	0.7 μm
Elementary gate width	200 μm	400 μm
Total gate width	400 μm	20 mm
Gate pitch	100 μm	40 μm

Fig. 10. Layout and device geometry of 2 and 50 gate fingers HEMT structures.

A very good agreement between simulations and experimental results confirms the validity of proposed methodologies and model parameters.

THERMAL ANALYSIS OF POWER HEMTS

After calibration of thermal properties the analysis of power multifinger HEMTs was performed. The above described structure with different thicknesses of SiC substrate and CuMo leadframe is used. The SiC substrate is usually grinded and polished to a lower thickness for the final assembly. Moreover, the chip is soldered to a package with thinner leadframe to improve heat transfer to the heat sink. Therefore, a 100 µm-thick SiC substrate and 300 µm-thick CuMo leadframe are used for the analysis. Boundary condition with the constant temperature of 50 °C is set on the backside of the leadframe. This represents an ideal heat transfer to a cooler during the steady state operation condition. Two different HEMT topologies with 2 and 50 gate fingers were investigated (Fig. 10). The analysis was focused on the influence of particular layers geometry and their thermal parameters on the thermal properties of HEMT.

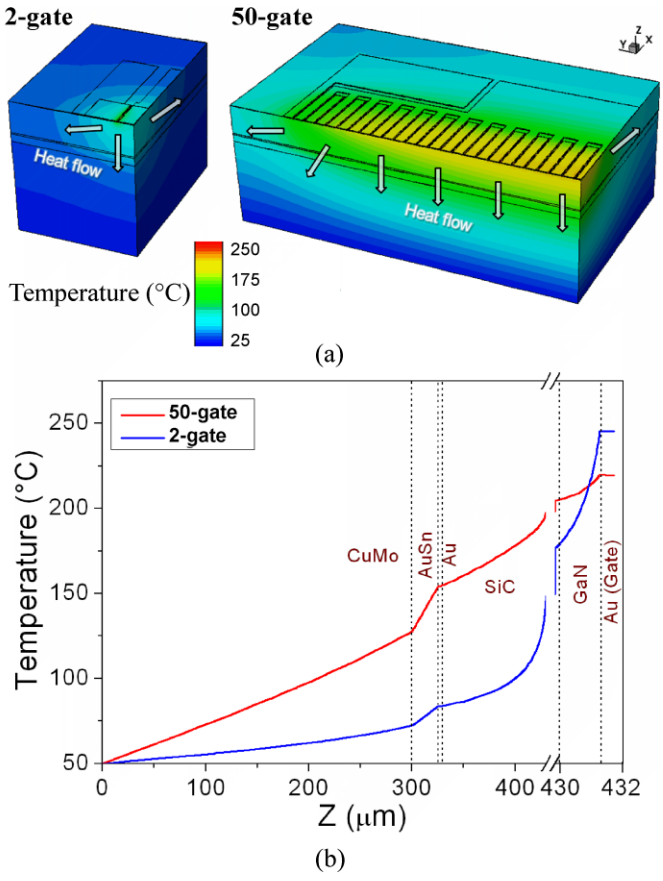


Fig. 11. (a) Temperature distribution inside HEMT structures. (b) 1-D temperature profile under the gate for HEMT structures with 2 and 50 gate fingers.

Fig. 11a shows temperature distribution for dissipated power 6 W and 80 W in 2- and 50-gate finger HEMT, respectively. The maximal temperature reaches about 250 °C for both structures. However, the normalized power dissipation per gate width unit is 15 W/mm and 4 W/mm for 2- and 50-gate HEMTs, respectively. It has to be noted that gate pitches and elementary widths are different for the two topologies. In case of the larger structure with 50-gate fingers, thermal crosstalk between gate fingers and higher active area dimensions reduce lateral heat flow and power dissipation capability [31]. Moreover, the reduced lateral heat flow increases temperature in the vertical direction compared to the 2 gates structure. One can clearly see from Fig. 11b that for the 2 gates structure the highest heat dissipation occurs in the top layers (GaN and SiC) while for the 50 gates structure the highest dissipated heat is mainly in the bottom layers (CuMo and AuSn).

The analysis of HEMT structures is focused on the influence of particular layers geometry and their thermal parameters on thermal properties and behavior. The investigated variables are thickness of layers Z and their thermal conductivities κ (Fig. 12 and Fig. 13).

Lowering the higher thermal resistive CuMo and AuSn layer thickness decreases HEMT temperature. Because of the

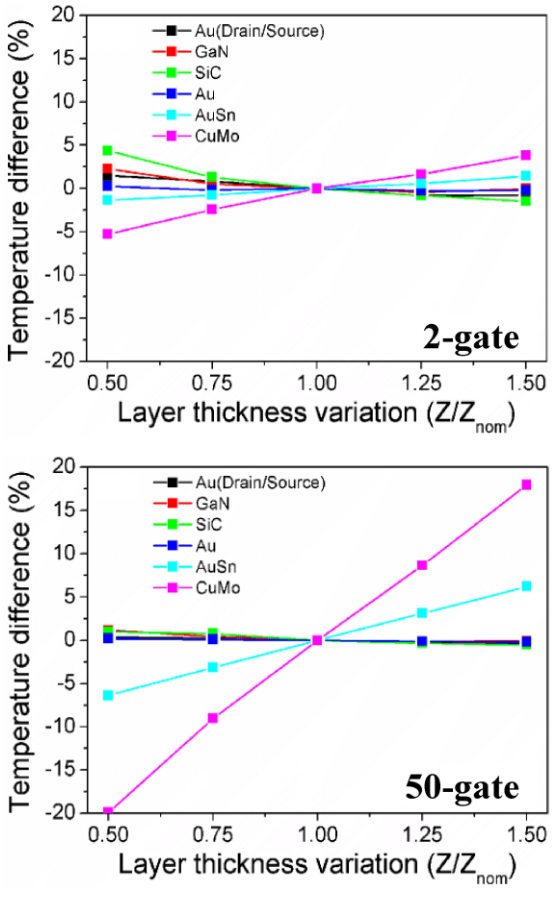


Fig. 12. Influence of layers thickness on HEMT temperature.

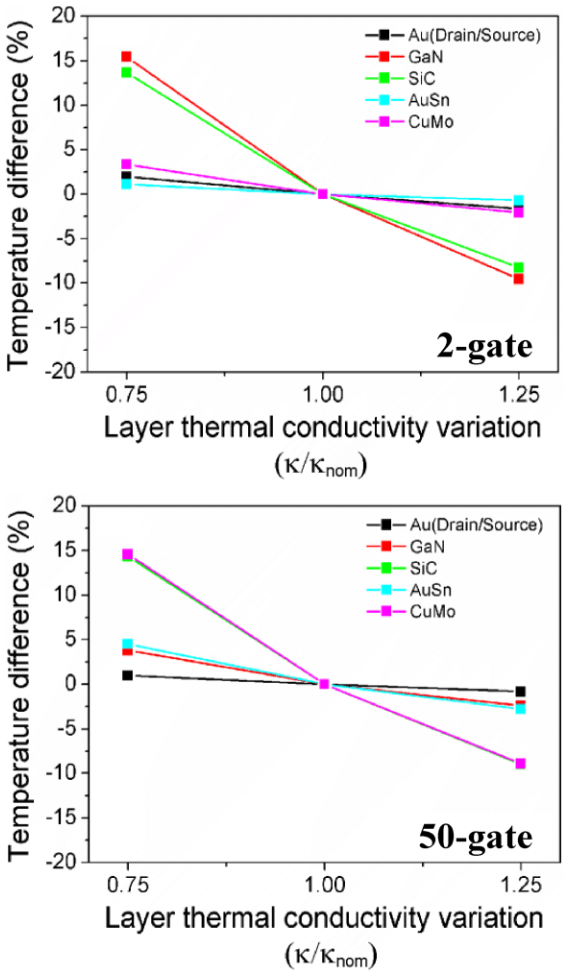


Fig. 13. Influence of layers thermal conductivity on HEMT temperature.

dominant vertical heat flow in the 50-gate HEMT, the impact of these layers on temperature is increased. Thinner SiC and GaN layers reduce lateral heat flow, increase vertical heat flow through low conductive AuSn and TBR layers (Fig. 14), and consequently increase HEMT temperature. As observed for the 50-gate HEMT, the reduced lateral heat flow diminishes the impact of SiC and GaN layer thickness on the temperature. Increasing the thickness of Au drain/source layers allows better cooling of the HEMT through the top metallization and therefore slightly decreases HEMT temperature. Higher thermal conductivity of all layers decreases HEMTs temperature (Fig. 13). GaN thermal conductivity has dominant impact for the 2-gate HEMT due to higher lateral heat flow in the top layers. The influence of the GaN thermal conductivity on the temperature of 50-gate HEMT with higher vertical heat flow is significantly lower. Impact of the AuSn solder thermal conductivity is slightly higher and the thermal conductivity of the CuMo leadframe becomes the most dominant. Influence of the SiC substrate is similar for both structures.

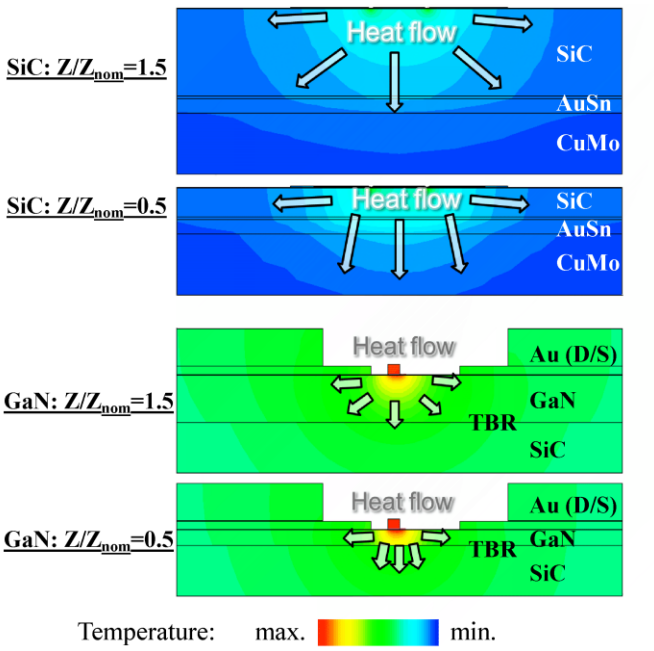


Fig. 14. Temperature distribution and heat flow inside HEMT structures for various thicknesses of SiC and GaN layers.

CONCLUSIONS

Several methods for on-chip temperature measurements of power AlGaN/GaN HEMTs grown on SiC substrate were presented. The device material thermal coefficients have been extracted from structure temperature distribution measured by micro-Raman spectroscopy and neighboring Schottky diode electrical measurement. The results have been validated by micro thermistor measurement. The well calibrated 3-D device model was used for thermal analysis of the multifinger power HEMTs. Different behavior has been observed, discussed, and explained for two HEMT structures. The effects of layers properties on the structure were investigated. The analysis of thermal behavior can help during design and optimization of power HEMTs. Our observations contribute to the on-going optimization of power transistor structures in respect to the geometry of layers design and their thermal parameters. Very good agreement between simulations and experimental results confirms the validity of the proposed methodologies and the model parameters.

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