A 24-28 GHz Doherty Power Amplifier with 4 W Output Power and 32% PAE at 6 dB OPBO in 150 nm GaN Technology

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*Abstract*—A 24–28 GHz two-stage GaN Doherty power amplifier is designed and characterized. At mm-wave frequencies, the low output impedance of the auxiliary transistor loads the Doherty combining network, which lowers the power added efficiency in back-off. In this design, a small periphery auxiliary transistor is used to increase the output impedance of the auxiliary transistor. The periphery ratio of the auxiliary and the main transistors is 77 %. Even though, compared to symmetric Doherty power amplifiers, the load modulation of the main transistor is reduced, this amplifier still achieves 32 % and 23 % power added efficiency at 6 dB and 9 dB output power back-off, respectively. Attributing to the small auxiliary transistor, the amplifier obtains a small signal gain of 19 dB. The maximum output power of the amplifier is 4 W with a peak power added efficiency of 42%.

*Index Terms*—5G, Doherty, GaN, mm-wave, power amplifiers.

1. INTRODUCTION

I

N the fifth generation (5G) mm-wave base-stations, antenna elements are closely spaced in an array due to the short wavelength. The power capability of such systems is thermal limited. Therefore, the power added efficiency (PAE) of power amplifiers limits the power capability of these systems, determining coverage and capacity for mm-wave base-stations. Furthermore, high order modulations, e.g., OFDM with up to 256 QAM are used in 5G communication system to get a high spectral efficiency. These signals have a high peak-to-average power ratio and thus require power amplifier (PA) with high power added efficiency (PAE) at high output power back-off (OPBO).

The Doherty PA is the most proven solution for improving back-off efficiency. The introduction of 5G in the mm-wave bands (24 – 29 GHz, 37 – 41 GHz) has spawned an interest in exploring Doherty amplifiers also at Ka-band.

Ka-band Doherty PAs in 45 nm CMOS SOI or in 130 nm SiGe BiCMOS technology have maximum output power in the range of 17 dBm to 28 dBm [1]. Their peak PAE are in the range of 20–40 %, and the PAE at 6 dB OPBO 14–33 %. Small signal gains (two-stage) are in the range of 15 dB to 19 dB. Ka-band Doherty PAs in 150 nm GaAs pHEMT technology have larger output power than those in CMOS/SiGe technology. The maximum outputs are in the range 25 dBm to 30 dBm [1]. The peak PAE are in the range of 25–35 %, and the PAE at 6 dB OPBO 14–25 %. Small signal gain (two-stage) are in the range of 10 dB to 13 dB [1].

There have also been several published Ka-band Doherty amplifiers in GaN technology. A 27–29.5 GHz three-stage Doherty PAs in 150 nm GaN technology can deliver maximum output power of 39 dBm [2] with PAE of 24 % and 19 % at 6 dB and 9 dB OPBO, respectively. The PA’s small signal gain is 30 dB. Another 21–24 GHz two-stage GaN Doherty PA [3] has maximum output power of 37 dBm with a better PAE than the previous one. The PAE are 30 % and 19 % at 6 dB and at 9 dB OPBO, respectively. It has a small signal gain of 17 dB.

Most published mm-wave Doherty PAs [2],[3], [5],[6], are symmetrical, i.e., the main and the auxiliary transistors at the output stage have the same gate periphery width. One of the published amplifiers is asymmetrical [4] where the periphery of the auxiliary transistor (8 × 60 *µ*m) at the output stage is twice as large as that of the main transistor (4 × 60 *µ*m). The purpose of using a large auxiliary transistor is to improve the PAE at back-off [4]. For that particular design, the obtained PAE of 20 % and 13 % at 6 dB and at 9 dB OPBO, respectively, does not indicate an advantage of having a large auxiliary transistor. Furthermore, the small signal gain of 13.6 dB is the lowest among Doherty PAs [2] – [6].

In contrast to the Ka-band GaN Doherty PAs [2] – [6], the Doherty PA presented here uses a small periphery auxiliary transistor, i.e., the ratio of the auxiliary and the main transistor’s periphery is less than 1.0. The obtained PA demonstrates state-of-the-art PAE at back-off and the highest small signal gain among published Ka-band two-stage Doherty PAs [2] – [6]. The reasons will be given in Section II.

1. *Circuit design and implementation*

## High frequency shunt loss

As shown in Fig. 1, an active transistor has parasitic drain-source capacitance, Cds, and shunt loss Rp, in parallel with the load impedance, Rload. The intrinsic shunt loss is often associated with losses of substrate and drain-extension of a power transistor, such as in an LDMOS transistor [7].



Fig. 1 Shunt loss due to the output parasitic of a power transistor.

At a high frequency, the impedance of Cds becomes relatively small, causing significant shunt loss via Rp. The efficiency degradation of a single-stage PA due to shunt loss is [7]:

$Eff\left(\%\right)=\frac{η\_{0}}{1+ω^{2}C\_{ds}^{2}R\_{p}R\_{load}}$ (1)

##### where $η\_{0}$ denotes the drain efficiency of a transistor operating in a certain class. For instance, $η\_{0}=78.5 \%$, when transistor operates in class-B.

The efficiency degradation is even worse in a Doherty PA, due to load modulation. For the main transistor at back-off power levels, the load Rload is multiplied by the load modulation ratio. According to (1) this load modulation degrades the drain efficiency of the main transistor by the same ratio. Furthermore, at the back-off power levels, the auxiliary transistor is in the off-state. The shunt loss of the auxiliary transistor is in parallel to the load impedance at the combining point (point A, as shown in Fig. 2). A large load modulation ratio means equivalently a large gate periphery of the auxiliary transistor. The RpCds product can be invariant to auxiliary transistor scaling. However, (1) shows that the efficiency degradation is proportional to $C\_{ds}^{2}$, so a larger auxiliary transistor causes higher loss.

Accordingly, for high frequency applications, it can be beneficial to reduce the load modulation ratio of a Doherty power amplifier to reduce the impact of shunt loss and to improve the back-off efficiency.

## Circuit design

The periphery of the auxiliary transistor needs to be selected carefully. Even though a small auxiliary transistor might be beneficial to minimize the loading of the power combiner network, it limits the current delivered by the auxiliary transistor, thus, reduces the load modulation of the main transistor and/or reducing high power gain and the maximum output power [8]. Hence, a trade-off between load modulation and output impedance must be made. The Doherty PA presented here has the periphery ratio of the auxiliary and the main transistor of 77%.

The PA is implemented in UMS GH15 process which is a 150 nm gate length GaN technology on SiC substrate. The technology addresses applications up to 40 GHz [9].

The Doherty power amplifier is designed with two amplifier stages in both the main and auxiliary branches, as shown in Fig. 1. In the main amplifier, the transistor size of the first and the second stage are 4 × 56 *µ*m and 6 × 94 *µ*m, respectively; and in the auxiliary amplifier the transistor sizes of the first and the second stage are 4 × 64 *µ*m and 6 × 72 *µ*m, respectively.

Two shunted inductors TL13 and TL15 tune out part of transistors’ parasitic capacitances. The impedance inverter is mainly composed of TL14in combination with the transistor output capacitances in parallel with TL13 and TL15. Also, C5 of 1.0 pF, used for DC-block, and C6 of 174 fF, contribute to the impedance inverter. The purpose of C6 is to reduce the influence of output impedance of the auxiliary transistor, thus, improving the back-off PAE [10]. During the design of the amplifier, it was found by simulations that C6 improves PAE less than 2 %. However, C6 blocks DC, and enables measuring the drain currents of the main and the auxiliary transistors separately. TL16 is used for impedance matching to 50 Ω.



Fig. 2. Schematic of the Doherty power amplifier.

The input impedance matching network for the first stage of main/auxiliary amplifier is made up of transmission lines and capacitor C1/C2, which transforms 100 Ω to a low input impedance for the first stage. Length difference between TL2 and TL1 (TL2 > TL1), as well as the periphery difference between the transistors in the first-stage create mainly a phase difference about 90° at the gates of the transistors at the last stage, to compensate the phase shift of the “impedance inverter”.

In the design, the periphery of transistors, the gate bias voltages, the capacitors’ size and the TLs’ length/width are chosen by harmonic balance simulations in Keysight ADS. Optimization is performed in ADS, targeting high output power, high peak and back-off PAEs, as well as a good impedance match at the input/output ports. Fig. 3 shows chip photograph of the designed Doherty PA. Chip size is 6.2 mm2.



Fig. 3. Chip photograph (periphery 3.1 mm × 2.0 mm).

1. Measurements Results

On wafer measurements were performed. Fig. 4 shows the measured and simulated gain and PAE at 27.5 GHz, as a function of output power. The measured small signal gain is about 19 dB, and the peak PAE is about 42 %. The maximum output power is 36 dBm. Measured PAE at 6 dB OPBO and 9 dB OPBO are 32 % and 23 %, respectively. In all measurements, DC supply voltage at drains is 20 V.

The simulated gain and PAE are lower than measured. It is due to the pulsed mode of the RF power and due to a process improvement in the fabrication that was not included in the model (improvement made after tape-out but before processing).



Fig. 4. Measured (solid line) and simulated (dash line) gain and PAE versus output power at 27.5 GHz.

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| TABLE IDoherty GaN PA (f>20GHz) |
| Ref. | Technology | Freq (GHz) | Circuit topology | Periphery ratio of aux. and main transistors (%) | Pmax (dBm) | Gain (dB) | Peak PAE(%) | PAE@6dB OPBO (%) | PAE@9dB OPBO (%) |
| [2] | 150 nm GaN-on-SiC | 27-29.5 | 3-stages | 100 | 39 | 30 | 30 | 24 | 19 |
| [3] | 150 nm GaN-on-SiC | 21-24 | 2-stages | 100 | 37 | 17 | 48 | 30 | 19 |
| [4] | 150 nm GaN-on-SiC | 24-28 | 2-stages | 200 | 32 | 13.6 | 21.7 | 20 | 13 |
| [5] | GaN | 27.5-29.5 | 2-stages | 100 | 35.6 | 18 | 25.5 | 22.7 | 19 |
| [6] | 100 nm GaN-on-Si | 26-29.5 | 2-stages | 100 | 33 | 13.7 | 36.2 | 30 | 19 |
| **This work** | **150 nm GaN-on-SiC** | **24-28** | **2-stages** | **77** | **36** | **19** | **43** | **32** | **23** |
| \*All values are given for a single frequency within the indicated frequency range |

Fig. 5 shows the PAE at maximum output power (0 dB OPBO), at 6 dB OPBO, and at 9 dB OPBO. As frequency is swept from 24 to 28 GHz, the PAE at the maximum output power varies from 23 to 41 %. Note that the peak PAE is slightly larger than the PAE at the maximum output power, as shown in Fig. 4, due to gain compression at maximum power. From 25 to 28 GHz, the PA demonstrates a good back-off PAE which vary from 25 to 32 % at 6 dB OPBO, and 19 to 23 % at 9 dB OPBO.

The maximum output power in the frequency range from 24 to 28 GHz is plotted in Fig. 6. Within this frequency range, the output power varies from 34 to 36 dBm. Correspondingly, the gain at the maximum output power varies from 11 to 13 dB. Fig. 6 plots also the gain at small signal input, at 6 dB and 9 dB OPBO. The small signal gain varies from 18 to 19 dB when the frequency is swept from 24 to 28 GHz. It can also be found that gain at 6 dB OPBO is less than the small signal gain at the same frequencies. But the difference is less than 1 dB, except at 24 GHz. The gain at 6 dB and 9 dB OPBO are approximately equal.



Fig. 5. Measured PAE versus frequencies at 0 dB, 6 dB, and 9 dB OPBO.



Fig. 6. Measured the maximum output power and the gains at maximum output power, at 6 dB and 9 dB OPBO, and at small-signal input.

Finally, the performances of Doherty-type GaN PA with a frequency higher than 20 GHz in the literatures are listed in Table I. The Doherty PA presented here exhibits the highest back-off PAE and a high small-signal gain (two-stages).

1. Conclusion

A Ka-band Doherty PA with a relatively small size of the auxiliary transistor is designed and characterized. Measurement shows that the designed PA achieves state-of-the-art back-off PAE and small-signal gain, thereby supporting the idea that mm-wave Doherty PAs can benefit from reduced size of the auxiliary transistor. In 5G millimetre-wave base-stations, the proposed technique improves the back-off efficiency, therefore, also the power capability of these systems.

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