



ECSEL Joint Undertaking

Electronic Components and Systems for European Leadership



Advanced RF Transceivers for 5G base stations based on GaN Technology



Project Acronym: 5G_GaN2

Type of action: ECSEL-RIA

Start date of the project: 01/06/2018

Duration of the project: 48 month

Grant agreement (GA) number: 783274

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Website: <https://www.5ggan2.eu>

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 783274. The JU receives support from the European Union's Horizon 2020 research and innovation programme and France, Germany, Slovakia, Netherlands, Sweden, Italy, Luxembourg, Ireland.



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Consortium members



UNIVERSITÀ
DEGLI STUDI
DI PADOVA



III-V lab





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Introduction

The fifth generation (5G) communications technologies will provide internet access to a wide range of applications: from billions of low data rate sensors to high resolution video streaming. The 5G network is designed to scale across these different use cases and will use different radio access technologies for each one. To support very high data rates 5G will use wide bandwidth spectrum allocation at mm-wave frequencies. The offered bandwidth at mm-wave frequencies (above 24 GHz) is more than 10 times larger than lower bands (sub 6 GHz). However, the move to mm-waves comes at a cost – increased path loss. This makes it extremely challenging to provide coverage at mm-wave frequencies.

A partial remedy is to use beamforming to direct the radio energy to a specific user. For some deployment scenarios beamforming is not enough and the output power must also be increased. A major challenge is to bring affordable, high-performance mm-wave active antenna arrays into production. There is currently a market pull for this systems but there exists a capability gap.

5G_GaN2 project will substantially lower the cost and power consumption and increase the output power of mm-wave active antenna systems. The maximum output power and energy efficiency results will be possible thanks to the use of advanced Gallium Nitride (GaN) technology. In addition, low-cost packaging techniques for RF and digital applications will be further developed to reach the cost and integration targets.

The capabilities of the developed technology will be shown in a set of demonstrators. The application driven demonstrators will be used to guide the technology development towards maximum impact and exploitation in the post project phase. The consortium spans the complete value chain: from wafer suppliers, semiconductor process integrators and system end users. In addition, key universities and research institutes guarantees academic excellence throughout the project.



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Project objectives

The major goal of the project was to demonstrate the capability to integrate heterogenous microwave dies in a single package. To reach this goal, the project is divided in work packages, which cover various activities such as:

- o Definition of specifications at system level
- o Development of front-end technology (integrated circuit, die)
- o Development of back-end technology for System in Package (die assembly)
- o Design of circuit and transistor modelling
- o Manufacturing and demonstrators' evaluation

Project results

Definition of specifications at system level

5G mm-wave base station system demonstrator properties have been defined and sub-system requirements have been specified. Document defines 5G mm wave BTS demonstrator specifications from die to SiP (System in Package) level. The report contains specifications for Front-End architecture and active antenna system architecture with very accurate figures. The subsystem analysis includes detailed electrical, RF (Radio Frequency), environmental and SiP specifications resulting into devices performance requirements. The definitions of the demonstrator vehicles, which are to be tested as part of manufacturing and evaluation objective were provided.



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Project results

Development of front-end technology

SweGaN AB has managed to develop performance-leading GaN-on-SiC epiwafers for RF and power devices. These wafers are based on buffer-free GaN-on-SiC epitaxial solution which show higher power density, higher efficiency, higher breakdown voltage and lower thermal resistance. The AlN/SiC interface is coined as out-of-plane compositional-gradient with in-plane vacancy ordering and can perfectly transform the in-plane lattice atomic configuration from the SiC substrate to the AlN nucleation layer (NL), avoiding formation of misfits and dislocations As shown on Fig. 1.

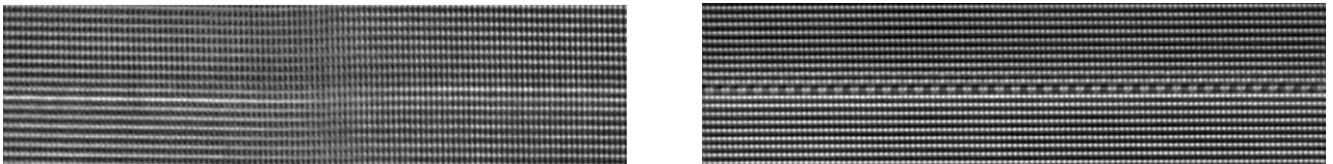


Fig.1: TEM images of the Conventional (left) and SweGaN proprietary growth interface.

The high-quality thin GaN is enabled by the transmorphic epitaxial growth of AlN nucleation layer on SiC substrate. 3.5% in-plane lattice mismatch (Δa) between GaN (0001) epitaxial layers and SiC (0001) substrates can be accommodated without triggering extended defects over large areas using a grain-boundary-free AlN NL. Defect formation in the initial epitaxial growth phase is thus significantly alleviated, confirmed by various characterization techniques. As a result, a high-quality 0.2- μm thin GaN layer can be grown on the AlN NL and directly serve as a channel layer in power devices, like high electron mobility transistors (HEMTs). The microwave performance was tested using HEMT grown on novel wafers. The concept of buffer-free structures is shown on Fig. 2.

Project results

Development of front-end technology (continue)

Barrier
UID GaN layer
C- or Fe-doped buffer
AlN NL
SiC substrate

Barrier
UID GaN layer
AlN NL
SiC substrate

Sample	QuanFINE		“Fe Buffer”	
Gate length (nm)	200	100	200	100
I_{DS-max} (A/mm)	0.95	1.06	1.04	1.14
Max g_m (mS/mm)	485	493	491	508
DIBL (mV/V)	13	50	10	40
SS (mV/dec.)	171	577	110	379
Off-state breakdown (V)	79	49	80	30
V_T (V)	-1.1	-1.5	-1.3	-1.5
R_{ON} (Q_{ref}) ($\Omega \cdot mm$)	1.78	1.47	1.68	1.36
R_{ON} (Q_{25}) ($\Omega \cdot mm$)	2.06	1.78	2.08	1.86
Dynamic R_{ON} (Increase %)	15.7	21	23.8	36.7
Z_1 (%) @ $V_{ds}=12.5V$	3.5	4	3.5	4
Z_2 (%)	11.5	14.6	13.9	17.8
f_T (GHz)	46	71	47	73
f_{max} (GHz)	114	129	117	130

Fig.2: Concept of conventional thick buffer (left) and buffer-free epi-structures (right).

Tab.1: Extracted figures of merit from DC, pulsed-I(V), and small signal measurements

The devices with the ‘buffer-free’ heterostructure show competitive DC and RF characteristics, as benchmarked against the devices made on a commercial Fe-doped epi-wafer. Peak transconductance of 500 mS/mm and a maximum saturated drain current of ~ 1 A/mm are obtained. An extrinsic f_T of 70 GHz and f_{max} of 130 GHz are achieved for transistors with 100 nm gate length. Pulsed-I(V) measurements reveal a lower current slump and a smaller knee walkout. The dynamic I(V) performance translates to an output power of 4.1 W/mm, as measured with active load-pull at 3 GHz. The results are summarized in Tab.1. These devices suggest that the ‘buffer-free’ concept may offer an alternative route for high frequency GaN HEMTs with less electron trapping effects. SweGaN intends to expand the capabilities to a mass production of the buffer-free GaN-on-SiC wafers in 12 months to 1000 pcs/month.



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Project results

Development of front-end technology (continue)

III-V Lab developed GaN HEMT devices for V-to E-Band applications. The aim was to study channel thickness impact on InAlGa_N HEMT devices and passivation thickness impact on InAlN HEMT devices as shown on Fig. 4. InAlGa_N structures have been fabricated using epitaxial growth at III-V Lab on 4 inches semi-insulating SiC substrate with sheet resistance between 270 and 310 Ohm/sq. The channel thicknesses of 100, 80 and 50 nm were compared. The results on channel thickness impact on InAlGa_N show better performances on 100 nm channel, low drain and gate lag on all structures, good robustness under high-temperature reverse bias reliability tests and operation of 6x50 μm devices at 45 GHz & 8x75 μm at 18 GHz. The results on passivation thickness impact on InAlN show that thinner Al₂O₃ layer yields lower PAE but higher RF gain and operation of 6x50 μm devices at 45 GHz.

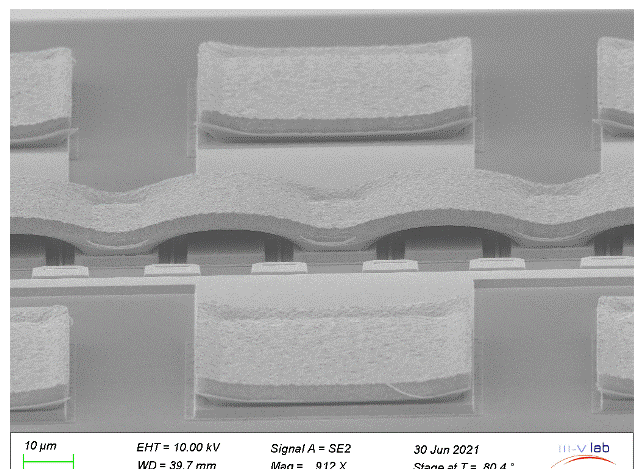
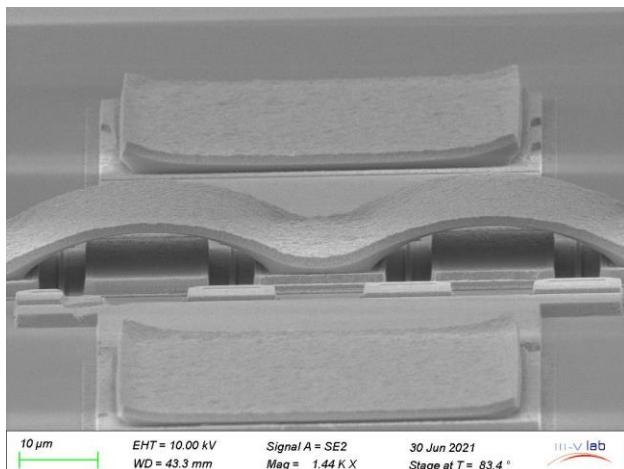


Fig.4: SEM images of InAlGa_N 80 nm channel structures with pillar-bridge interconnects (left) and InAlN structure pillar-bridge interconnects (right).



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Development of front-end technology (continue)

The development of CMOS compatible GaN on Si is a significant challenge for large scale production with low cost. In less than 4 years, LETI CEA Tech has set up a 200mm GaN on Si transistor, compatible with CMOS technology, demonstrating reduction of RF losses after epitaxy down to $-0,28\text{dB/mm}$, efficient thermal stack for power amplification, implanted ohmic contact with low contact resistance ($RC \sim 0,15\text{Ohm.mm}$) well suited for high frequency applications and feasibility of this technology with CMOS compatible process (gold free, lift-off free, planar, particles management...) that results high yield and excellent uniformity. On external low losses epitaxy, a good large-signal performance ($\text{PAE} > 40\%$ at 28GHz) has been demonstrated on fabricated devices despite of limited large signal performance ($\text{PAE} \sim 28\%$) on their own epitaxy with encouraging DC, pulsed and S_{ij} measurements ($f_T \sim 65\text{GHz}$, $f_{\text{max}} \sim 128\text{GHz}$ with $L_G = 150\text{nm}$). Further development on RF losses, trapping effect, gate and contact process will allow to reach higher performance.

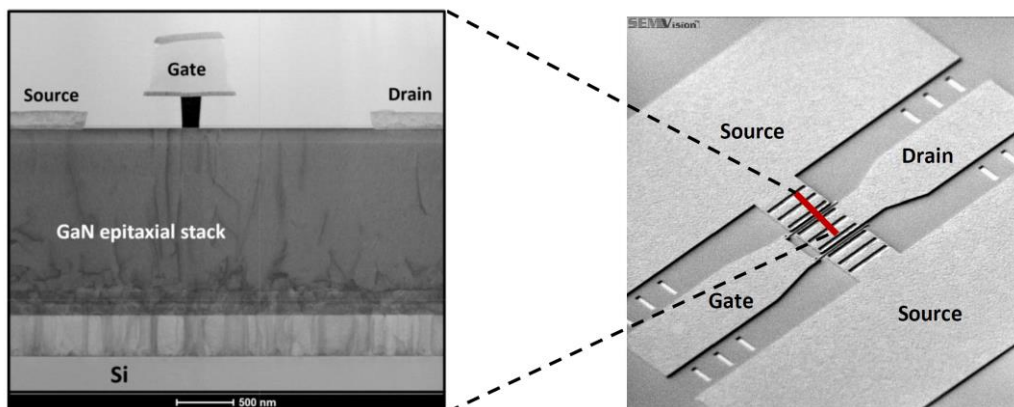


Fig.4: CMOS compatible GaN on Si in STEM cross-section (left) and top view (right).



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Project results

Development of back-end technology for System in Package

FOWLP integration of GaN and GaAs RF chips featuring large frontside topology, air bridges, low thickness ($\sim 100\ \mu\text{m}$) relative to the EMC, Au backside coating for 5G telecommunications has been successful. SiPs embedding HPA and LNA III-V chips were manufactured for 5G transceivers operating at 28GHz such as shown on Fig. 5. HPA thermal management improvement has been achieved through EMC laser ablation, and subsequent Cu heat spreader plating. Original wafer configuration has been proposed including a limited molded area enabling to limit die shift even when using mask aligner. Signal losses of 0.1 dB/mm at 30GHz and 0.4dB/mm at 60GHz have been successfully measured in SiP-like environment (RDL 50 ohm lines).

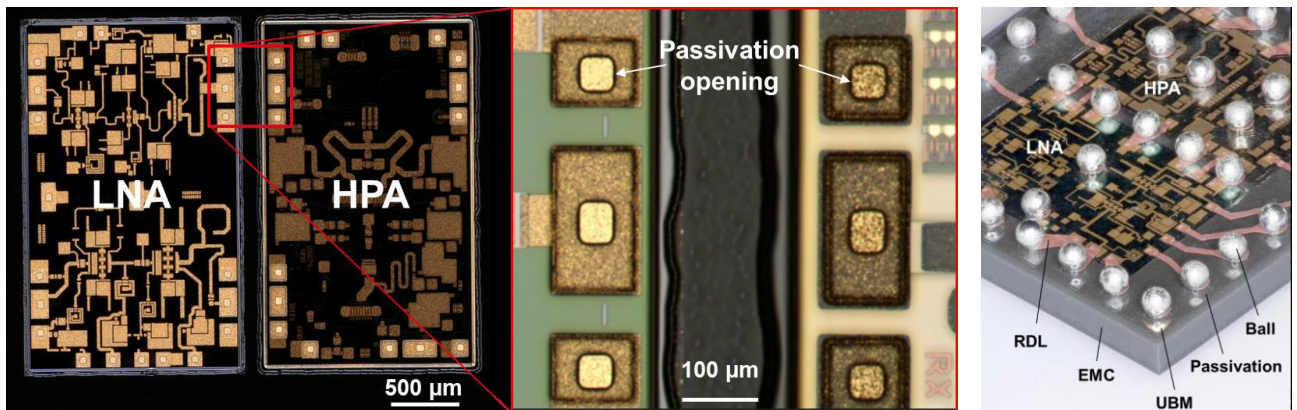


Fig.5: Images of LNA and HPA chips (left) with passivation (middle) and MMIC SiP with solder balls (right).



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Project results

Development of back-end technology for System in Package (continue)

United Monolithic Semiconductors (UMS) developed and tested several front-end modules including High Power Front-End (HPFE) module for small MDU/SFU transceivers, High Power Front-End module for base stations (Fig. 3) and 39GHz GaN HEMT High Power Front-End module for 5G transceivers. Next step will be the assembly on FC BGA and FOWLP package for 39GHz GaN HEMT High Power Front-End module.

It has been proven that UMS GaN technologies offer high-power performances at mm-wave frequencies for 5G HPFE, mixed MMIC technology offers an interesting trade-off between performances, size and cost. Moreover, it has been clarified that advanced packaging technologies enable new active antenna architectures and heterogeneous integration offers state-of-the-art performances for 5G RF & mm-wave applications.

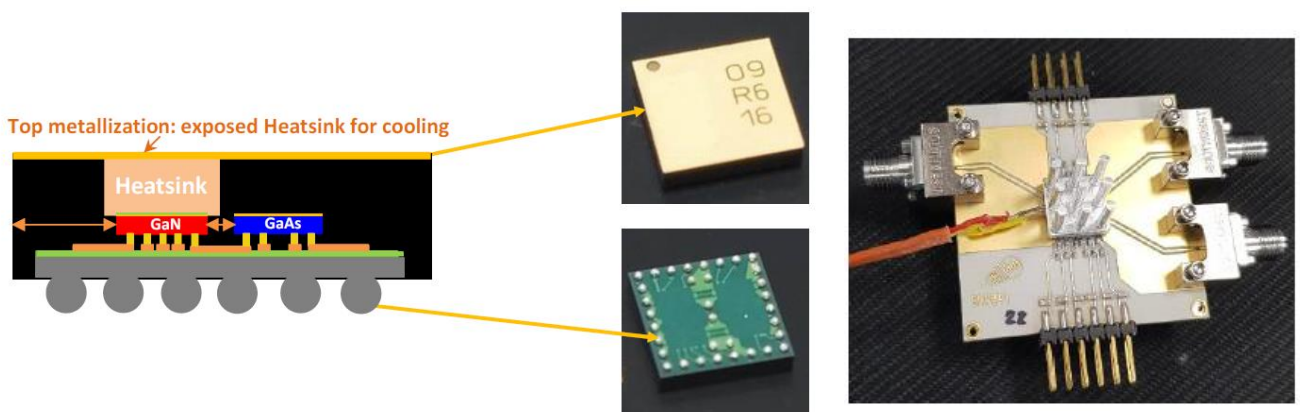


Fig.3: Full SiP integration for High Power Front-End module for base stations.



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Project results

Development of back-end technology for System in Package (continue)

Single pole double throw and low noise amplifier (LNA) on SOI for 5G applications demonstrator has been successfully fabricated and characterized. New silicon blocks for the 39-GHz 5G/SATCOM SiP demonstrator have been introduced. The results have been comprised with the same functionalities on GaAs or GaN technology with main targets towards silicon RF performance limits, power consumption, integration improvement, cost optimization and creation of hybrid GaN/Si RF front-end module as shown on Fig. 6 with core size of 1.3 mm x 1.2 mm (1.56 mm^2) and good RF performance. The next step will be full implementation with GaN high-power amplifier.

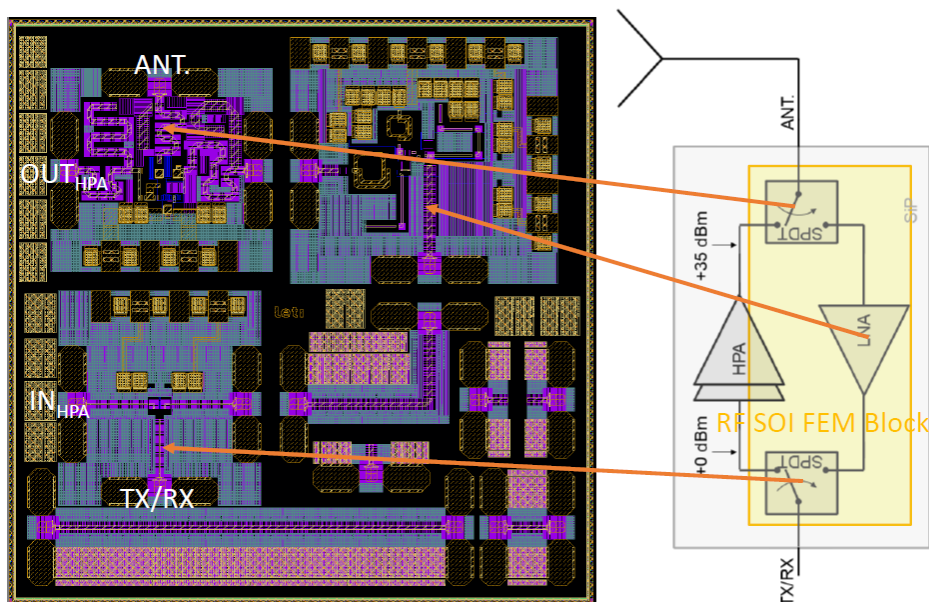


Fig.6: RF silicon on insulator front-end module block.

Project results

Development of back-end technology for System in Package (continue)

A Ka-band Doherty PA in 150 nm GaN-on-SiC technology has been successfully designed and characterized, where state-of-the-art performance was demonstrated. At millimeter wave, the Doherty power amplifier benefits from reduced size of the auxiliary transistor in terms of PAE at back-off and gain. Two-stage 24-28GHz high power amplifier based on 0.15 μm GaN technology with transistor's size of $6 \times 72\mu\text{m}$ (aux.) and $6 \times 94\mu\text{m}$ (main) in the output stage has been fabricated (Fig. 7) and tested. This Doherty PA can be used in a 5G millimeter wave system, improving the power capability of the system.

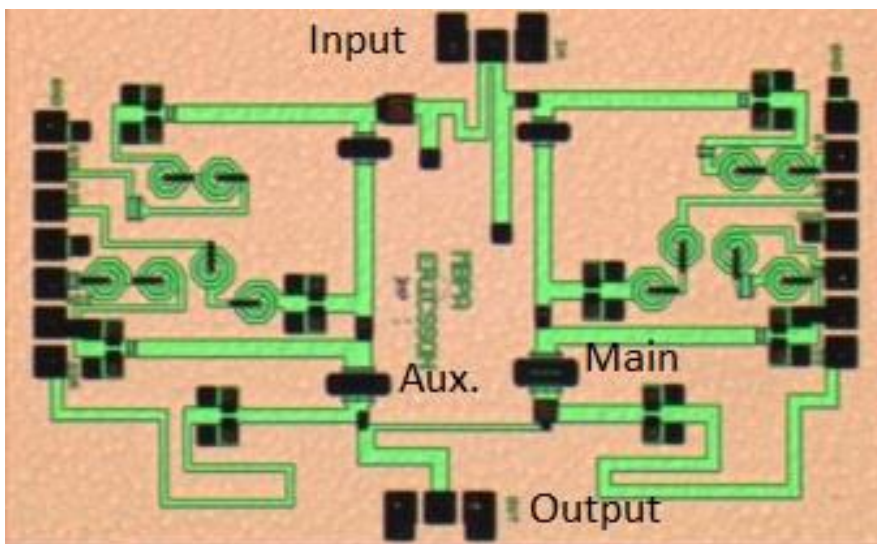


Fig.7: Doherty 24-28GHz high-power amplifier.



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Project results

Design of circuit and modelling of transistor

At IAF the researchers have been working on advanced 100 nm GaN HEMT technology for 5G E-Band backhaul applications. Specifically on 100 nm technology approach and consequentially transistor modeling and MMIC design. The technology has been successfully implemented and marked suitable for Ka-Band, E-Band and W-Band applications. HEMT devices using the new approach have been successfully designed, fabricated and characterized for operation at 38 GHz frequencies. Subsequently, an E-Band power amplifier and E/W-Band low-noise amplifier have been designed, fabricated and successfully tested (Fig.8).

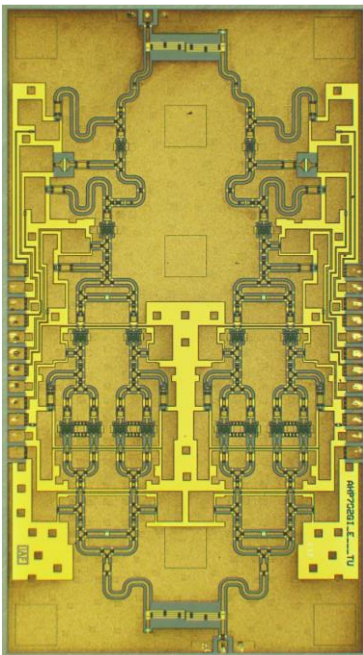
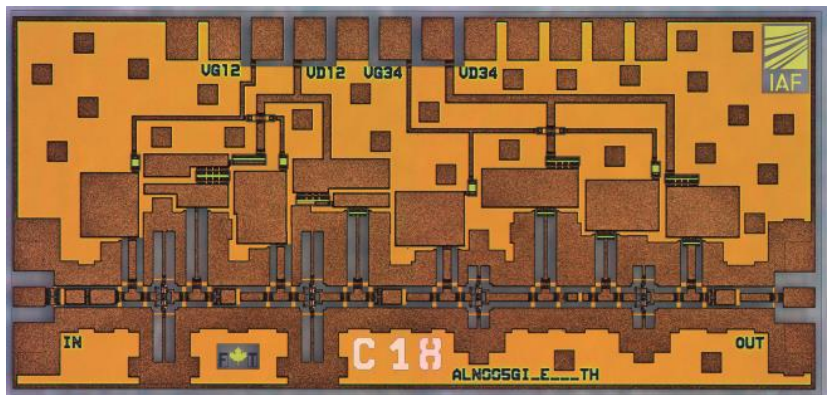


Fig.8: Balanced 4-stage, 1 W, E-Band power amplifier die with size of $4 \times 2.25 \text{ mm}^2$ (left) and 4-Stage Low-Noise Amplifier, 3 dB, E/W-Band low-noise amplifier with size of $2 \times 1 \text{ mm}^2$ (right).





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Project results

Design of circuit and modelling of transistor (continue)

In the frame of the project, TESAT, MEC, SENCIO and UMS designed, fabricated and tested a 20GHz 4W power amplifier in SMD Plastic Package for SatCom applications. 150nm GaN HEMT technology based on SiC substrate has been used which is well-suited for a wide range of applications up to 35GHz. RF MMICs are to be integrated with other RF components and DC control electronics while for established space applications, hermetic sealing is requested. Due to the absence of atmosphere, the most relevant thermal path is given by the backside metallization. These RF modules are integrated with additional control and interface circuits on regular multilayer PCBs to the final product. Based on CAD and thermal simulation models a detailed investigation on thermal situation has been carried out and compared for SMT plastic package (for PCB mounting, Fig. 9) and Hybrid package (for hermetic sealing). The measured results obtained are in line with the predicted and expected behavior - i.e. device models are mature.

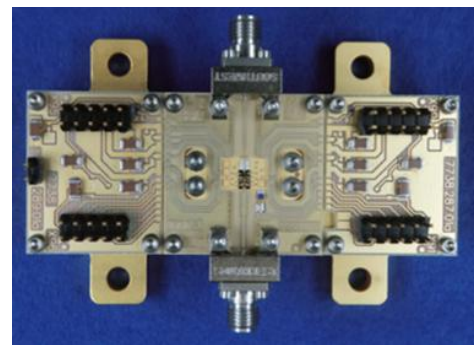
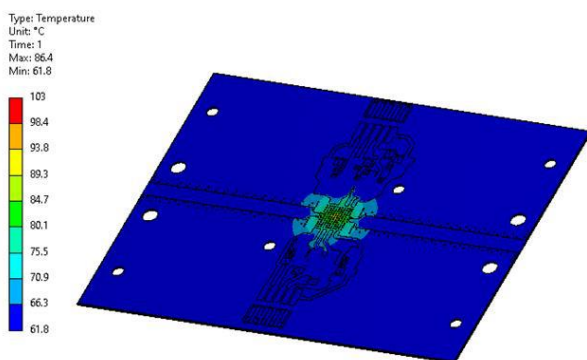


Fig.9: Heatmap “SMT package” PCB surface (left) and test module with MMIC die mounted on representative heatsink (right)



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Project results

Design of circuit and modelling of transistor (continue)

Thales designed, fabricated and tested in plastic QFN (SENCIO) a new Ka Band Front-end SiP including two MMICs using UMS GH15-10 process. Main RF performances have almost been achieved with the first Run. Total power consumption of board match with specifications at system level and EIRP (Effective Isotropic Radiated Power) has been improved compared to previous solution. All the tools and software developed for testing have been validated. Several thermomechanical and humidity tests will be performed on the PCB to check if delamination or cracks will be observed at the end of the cycling tests. New Design Kit should improve stability margin in Ka band and the frequency shift should be corrected. Run 2 design work will mainly be to improve power performances over [27-31] GHz frequency band and achieve a higher isolation level on the Ka band switch.

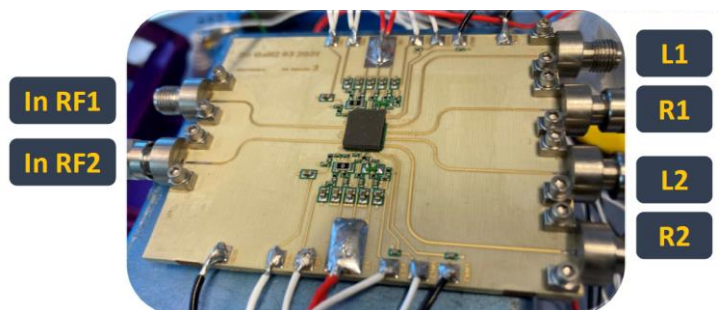
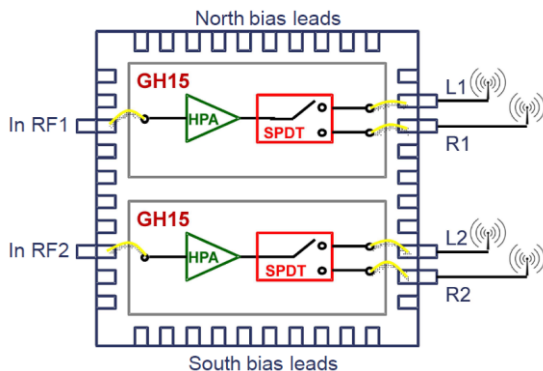


Fig.10: New Ka Band Front-end SiP including two MMIC (left) and evaluation board designed by Thales (right)



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Dissemination activities

Workshops organized within EUMW 2021 event

The Workshops have been organized at one of the most remarkable events in microwave world, European Microwave Week (<https://www.eumw2021.com/>). This event takes place annually and joins researchers and industrial partners in the field not just from the Europe but from the whole World. Among the Workshops there were three significant conferences and industrial exhibitions. It has been an honor for the speakers at the workshop to actively participate on such event. The event has been postponed from initial date due to problematic travel situation during the pandemic years 2020 and 2021.

The speakers at Workshop on material research have presented the latest research results achieved on material research. The session has been opened by Philippe Fellon (UMS) as the project coordinator and the whole session has been chaired by Hermann Stieglauer (UMS) afterwards. The speakers mostly presented technology approaches, material research and characterization techniques exploited for optimization of device fabrication for microwave application essential for achievement of proposed goals in 5G_GaN2 project. The delegates in audience stir up a live discussion after each presentation leading to interesting conclusions.

The speakers at Workshop on devices and applications presented the latest research results achieved on devices and applications. The session was continuing morning session aimed at material research and the whole afternoon session has been chaired by Jaroslav Kovac (STUBA). The speakers presented device systems for microwave signal processing, mostly amplifiers, and their appropriate packaging technology acting as demonstrators for application in 5G networks essential for achievement of proposed goals in 5G_GaN2 project.



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Dissemination activities

Publications summary

During 4 years of project run, 5 papers in peer reviewed scientific Journals and 33 contributions at Workshops and Conferences have been published including Workshops organized by consortium (Fig. 11).

Peer reviewed scientific journal papers:

- [1] Chvála A, et al. in ASME. J. Electron. Packag. 141(3):031007-031007-7 (2019)
doi:10.1115/1.4043477
- [2] Kanyandekwe J., et al. in Journal of Crystal Growth 515:48–52 (2019)
doi:10.1016/j.jcrysgro.2019.03.007
- [3] Florovič M., et al. in SEMICONDUCTOR SCIENCE AND TECHNOLOGY 36(2) (2021) doi: 10.1088/1361-6641/abd15a
- [4] Bao M., et al. in IEEE Microwave and wireless compound 31(6) (2021)
doi: 10.1109/LMWC.2021.3063868
- [5] Florovič M., et al. in Electronics 10(22):2738 (2021)
doi: 10.1088/1361-6641/abd15a



Fig.11: Presenters at Workshops on EUMW2021 event



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Project events

Project meetings and general assemblies

The coordination of project activities were running through group meetings and general assemblies of consortium members during the whole project execution. The more specific project tasks have been assigned to consortium members on June 26th 2018 at Kick-off meeting in Paris. Three important meetings have been organized in person during 2018-2019 period and last five meetings were organized virtually during 2020-2022 because of complicated pandemic situation around the world. The seriousness of the project implementation has demanded amendment of project duration from 36 to 48 month. The project has been finished on 31st of May 2022 and will be revised by EC in September 2022.



Project 5G_GaN2 operational team at Kick-off meeting in Paris